Implementing a Xilinx Project

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Apr. 23, 2012

So, you've synthesized your VHDL design and now it's time to implement it, generate the bitstream file, and download the bitstream into the FPGA to configure it according to your design. This document will take you through that process using the Xilinx and Digilent Adept software:

- Implementing your design and verifying your design's pin constraints.

- Generating a bitstream file.

- Preparing the FPGA board (Digilent Adept).

- Downloading a bitstream into the FPGA board (Digilent Adept).

I assume you have a synthesized design upon which you've performed behavioral simulation.

1 Implementing a Design and Verifying Pin Constraints

Pin constraints are necessary so that the inputs and outputs of your design are connected to the appropriate pins of the FPGA chip on the Nexys 2 board. Without these constraints, the Implement Design tool will assign whatever pins are most convenient for it to your design's inputs and outputs. These pin constraints are defined by a series of attribute statements in your VHDL source file. Here's a short example:

```
attribute LOC : string;
attribute LOC of mclk : signal is "B8";
attribute LOC of pdb : signal is "R10 P10 R11 N11 T12 P13 R13 R14";
```

Do not modify these VHDL statements. At best, your design won't work. At worst, you'll damage the Nexys 2 board and be expected to pay for its replacement.

1. Change the Design view to Implementation and highlight your top-level module file in the Hierarchy display.

2. If you haven't already done so, synthesize your design by double-clicking the Synthesize tool in the Processes window. Correct any errors.

3. To implement your design, double-click the Implement Design tool in the Processes window. Correct any errors.

4. Bring the Design Summary window forward and select the Pinout Report. Scroll through the report and confirm that all location constraints were honored. If they were not, go back and correct the errors. After correcting any errors, run Cleanup Project Files (under the Project menu) and re-run the Synthesize and Implement Design tools.

   Do not proceed until the Pinout Report is correct.

2   Generating a Bitstream File

You should confirm that you have selected the correct Project Settings before proceeding. To do so, select Design Properties from the Project menu in Project Navigator. The following fields should have the following values — Family: Spartan3E; Device: XC3S500E; Package: FG320; Speed: -5. If you change any of these fields, run Cleanup Project Files (under the Project menu) and re-run the Synthesize and Implement Design tools.

1. You should have a successfully implemented design, and verified the design's pin constraints, before proceeding.

2. Right-click the Generate Programming File tool and select Process Properties. Click the Startup Options tab. Set the FPGA Start-Up Clock to JTAG Clock. Click the OK button.

3. Double-click the Generate Programming File tool to generate your design's bitstream file.

3   Preparing the FPGA Board

1. Place the Nexys 2 board flat on a horizontal surface so that the large DIGILENT name near the center of the board is facing you. From this board orientation, there is a power switch in the upper-lefthand corner of the board. Ensure that the switch is in the off position — toward you.

2. Along the board's left edge, near the bottom of the edge and between the board's serial port and PS/2 connectors, there is a USB mini connector port. Connect the corresponding end of the USB cable to this port. The USB symbol on the cable end's "handle" should be facing you.

3. Connect the other end of the USB cable to a live USB port on your workstation.

4. Flip the power switch to the on position. A red LED below the switch should illuminate.

   Reverse these steps to prepare the board for storage.

5. Start the Digilent Adept software: From the Start menu, choose Digilent, Adept, Adept. The software should display Nexys2 in the Product field.

   Should you want to test the board, Click the Test tab within the Digilent Adept tool's window, and press the Start Test button. Within a few seconds, the four 7-segment displays should alternately flash PASS and 128, and a yellow LED to the right of the red LED should illuminate. When you're finished with the test, press the Stop Test button.

4   Downloading a Bitstream

1. Select the Config tab within the Digilent Adept software.

2. To the right of the FPGA field, press the Browse button and browse to the .bit file that you want to load into the FPGA. Press the Program button to load the bitstream file into the FPGA.

   We won't be using the PROM field.

   The yellow LED will extinguish while the bitstream is being loaded into the FPGA. Once loading has completed, the yellow LED will illuminate.

3. You're now ready to use the FPGA.