

# Integrated Circuit Technology

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## 1 Administrivia

### Announcements

### Assignment

Read 3.1–2.

### From Last Time

NAND gates, two-level implementation, parity.

### Outline

1. Terminology.
2. Transmission gates.
3. CMOS.

### Coming Up

Combinational logic design process and simulation.

## 2 Terminology

1. Today's important logic families: TTL, CMOS, LVTTTL.

Voltage, current, power, speed.

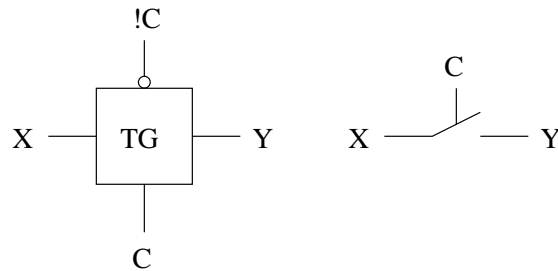
2. Fan-in, fan-out.
3. Noise margin. Where does noise come from?
4. Power dissipation. Who cares? Extended battery, device life.
5. Propagation delay. Don't forget about wires: on-chip and off-chip.

Delay may be asymmetric:  $t_{pht}$ ,  $t_{plh}$ . Max of both:  $t_{pd}$ .

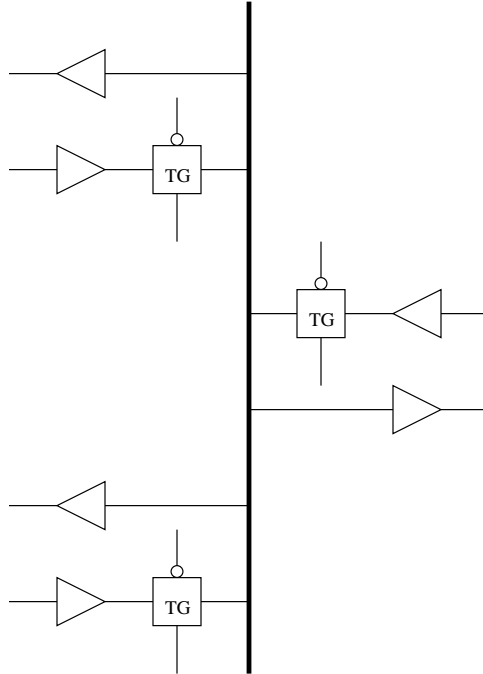
6. We'll only examine *positive logic* and *transport delay*.

## 3 Transmission Gates

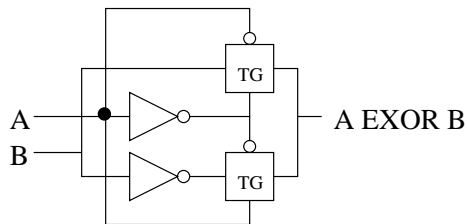
An electronic switch:



Typically used to enable writes onto a bus. For examples, two CPUs sharing a memory bus. Bus arbitration.



Can be used in more crafty ways: viewing an EXOR as a “conditional inverter:”



Eight transistors; two gate delays.

The standard NAND implementation requires four gates (16 transistors) and has a propagation delay of three gate delays.

## 4 CMOS

### 4.1 CMOS Transistors

1. N-type transistor:

(a) Passes GND well.

(b) Degrades Vdd.

(c) Normally open switch.

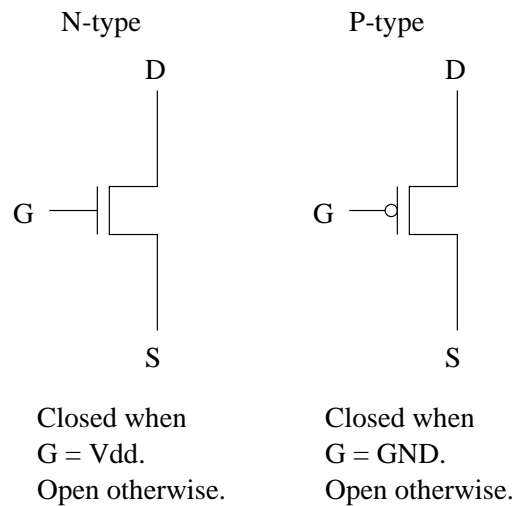
2. P-type transistor:

(a) Passes Vdd well.

(b) Degrades GND.

(c) Normally closed switch.

Diagrams:

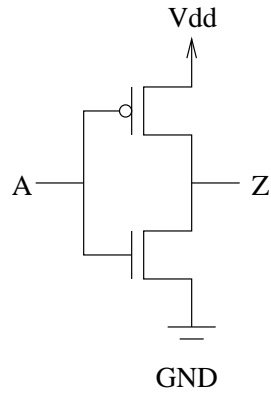


1. Terminals: gate, drain, source.

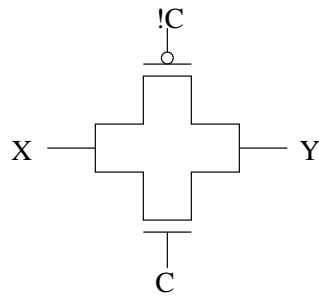
2. High capacitance on the gate.

## 4.2 CMOS Logic Gates

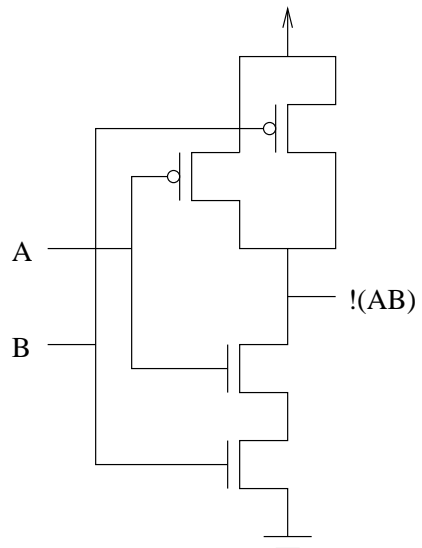
A CMOS inverter:



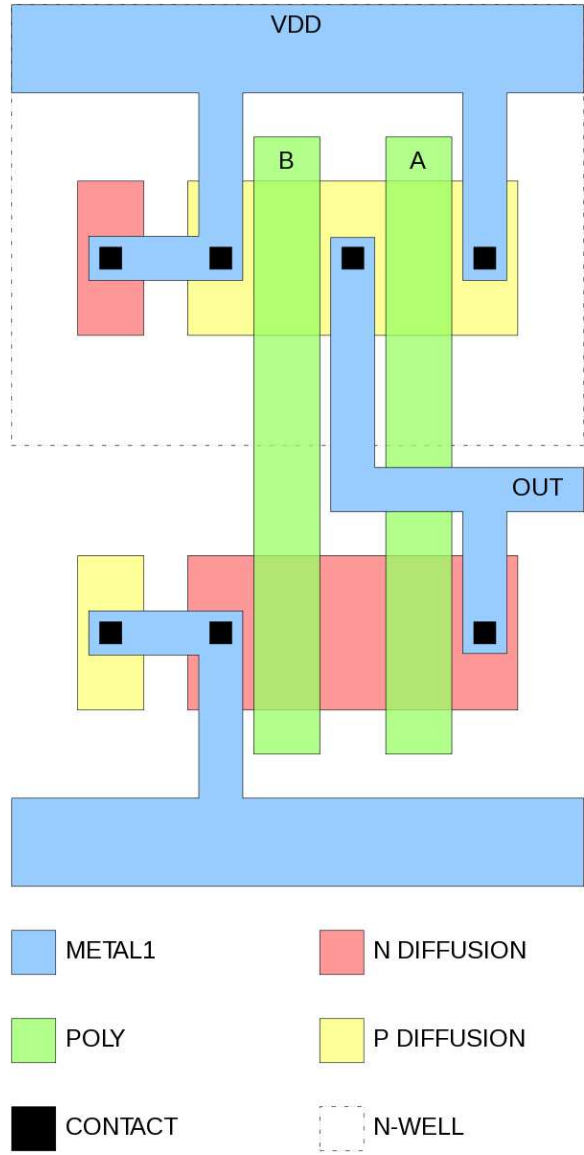
A CMOS transmission gate:



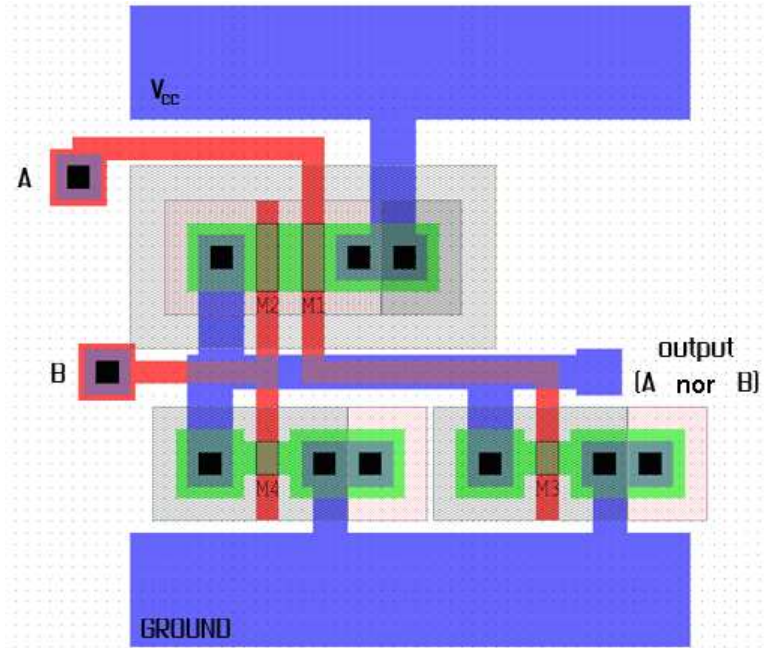
A CMOS 2-input NAND gate:



Layout of a CMOS 2-input NAND gate:



Layout of a CMOS 2-input NOR gate:



What determines power dissipation? Switching frequency.

Why transport delay isn't a good model: It takes time to move the charge on the gate. This is correctly modeled with inertial delay.

Structure of a NOR gate?