Homework VI

Tom Kelliher, CS 240

50 points, due Apr. 18

1. 5-18.

   Additionally, implement your design in VHDL. Then, download your design to one of the FPGA boards in the X Lab, run my test program to test your circuit, and report the result. Submit the state diagram, state table, VHDL source code, and the report of your result.

   Note carefully that my test program provides an input to your circuit and then samples the output of your circuit **before** clocking your circuit. (Refer to the program's source code.) This means that your circuit's current output value should correspond to the current input, behavior consistent with a Mealy machine. The comments in the test program's source code regarding the active low reset signal should be ignored.

2. 5-24. One modification: the asynchronous `RESET` signal is to be **active low**.

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I won't make the Xilinx boards available until you're ready to use them. Please give me advance notice of when you plan to begin using the boards.