Decoders, Encoders, and Muxes, Oh My!

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1 Administrivia

Announcements

Assignment

Read 4.1–4.2. Review mostly; background for carry lookahead.

From Last Time

Combinational design example.

Outline

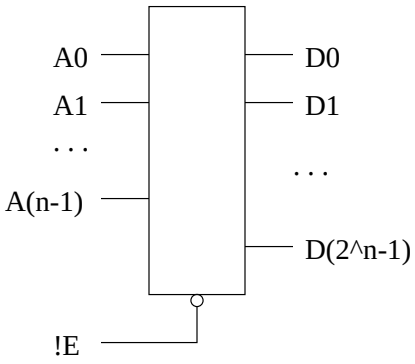
1. Decoders
2. Encoders
3. Muxes

Coming Up

Lower bound for addition. Fast addition algorithms.

2 Decoders

Block diagram (diagram a 3-8 decoder):



A circuit with n inputs. The inputs are interpreted as a binary number and used to select one of 2^n output lines.

1. Most common use: Address decoders for RAMs and register files.

2. Decoder expansion example: design a 5-to-32 using 5 3-to-8 decoders.

3. Example use: Design a BCD to seven segment decoder using a 4 to 16 decoder and OR gates.

3 Encoders

Inverse of a decoder: 2^n inputs; n outputs.

1. What happens if multiple inputs are high?

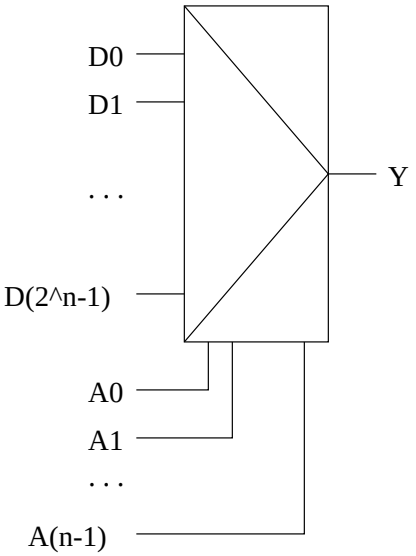
2. Most common uses: priority encoders for interrupt controllers; "hit" logic for caches.

3. Design example: Four input priority encoder with a "Valid" output.

4 Muxes

Used to select one of 2^n inputs. One way switch.

Block diagram (draw a 4-1 mux):



1. Most common uses: RAM, register file data selection circuits; Boolean function generators.

2. *What's a quad 2-1 mux?*

3. Design example: Implement a three input Boolean function using an 8-1 mux. No additional logic.

   Four input Boolean function using an 8-1 mux and an inverter?

   Five input Boolean function?