Final Exam Review

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1 Administrivia

Announcements

"Homework" due Friday.

Assignment

From Last Time

Virtual memory.

Outline

1. Review for final.

Coming Up

Final.

2 Review for Final

- Chapters covered: 2–7.
- Refer to previous reviews for earlier material.
- Slight bias toward more recent material, but coverage will be fairly even.
- Final exam format:
  - 8 short answer questions. Each 15 points.
  - Two "essay" questions. Each 40 points.

1. Pipelining:
   (a) Changes to datapath, control
   (b) Hazards: structural, data, control. Penalties, solutions.
2. Superscalar execution:
   (a) IPC
   (b) Widening the *entire* datapath.
   (c) Applicability.
   (d) Types of data dependencies. True, false dependencies. Removal of false dependencies: register renaming.
   (e) Out-of-order execution, in-order completion.
3. Caches:
   (a) The memory hierarchy.
   (b) Exploiting program locality properties. Advantages of using caches.

(c) Cache types: direct mapped, set-associative, fully-associative.

(d) Address partitioning: tag, offsets.

(e) Ideas behind direct-mapped caches. Analysis of direct mapped caches.

4. Virtual memory:

   (a) Mapping between virtual address space and physical address space (memory and paging device).

   (b) Locality, advantages.

   (c) Requirements:

      i. Kernel support: page fault handler, page placement and page replacement policies.

      ii. MMU support: valid/invalid bit, reference bit, dirty bit, read/write bit.

      Exceptions generated: memory fault (unmapped page), page fault (page not in memory), write on read-only fault.

      iii. CPU support: Instructions must be re-startable.

   (d) Page fault sequence (memorize all 147 steps).

   (e) Demand paging performance: effective access time.

5. Important earlier material:

   (a) Performance comparisons.

   (b) Carry lookahead adders.

   (c) MIPS programming.

   (d) Function unit design.

(e) Single- and multi-cycle implementations.