

Single- and Multi-Cycle Implementations

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Mar. 26, 2004

1 Administrivia

Announcements

Assignment

From Last Time

Single-cycle implementation.

Outline

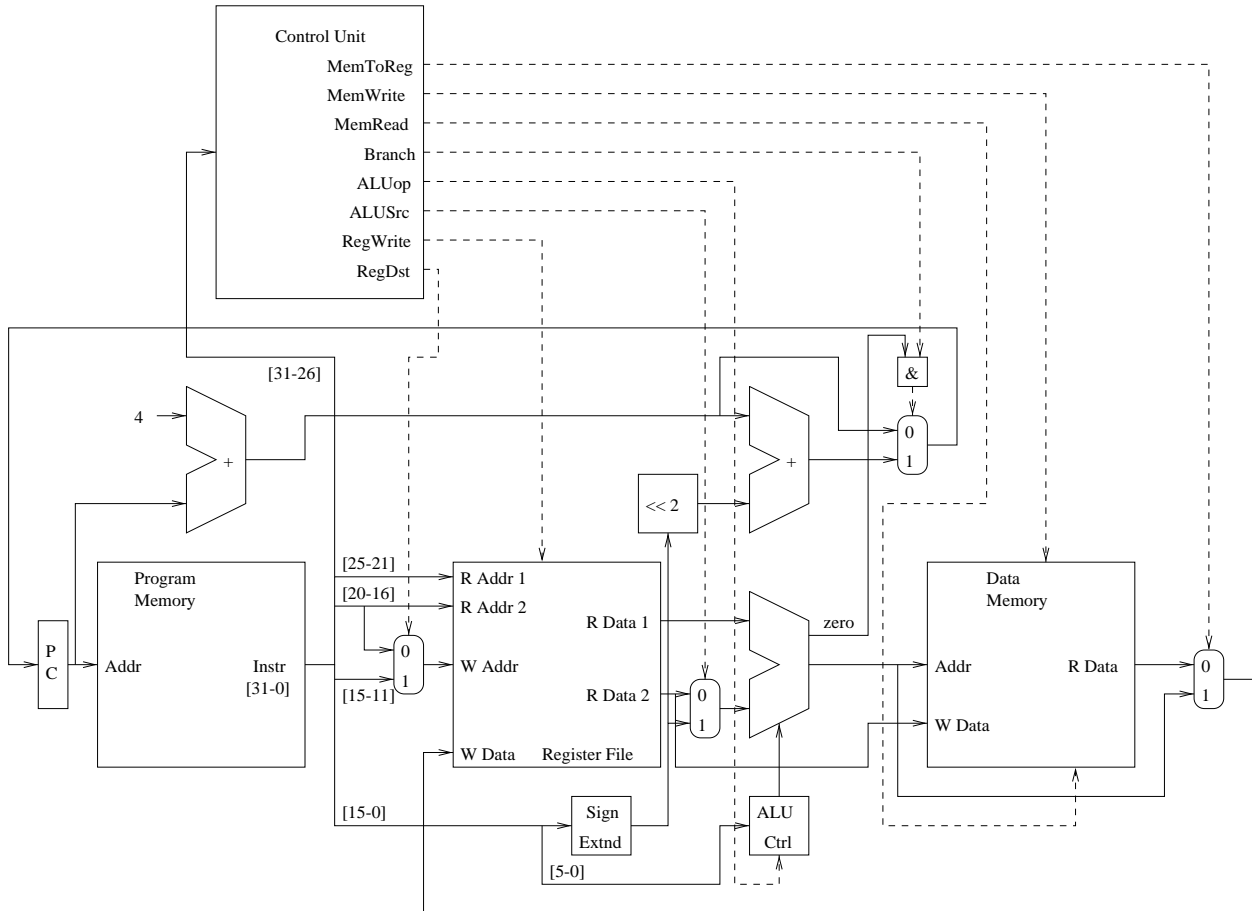
1. Adding an instruction.
2. Disadvantages of the single-cycle implementation.

Coming Up

More on multi-cycle implementation.

2 Adding an Instruction

How do we go about adding support for the jump instruction? What changes do we make to:



3 Disadvantages of the Single Cycle Implementation

Assume the following:

1. Memory read/write: 2 ns.
2. ALU and adders: 2 ns.
3. Register file read/write: 1 ns.

4. All other delays are zero (not practical).

How much time is required for each instruction? (Emphasize notion of longest path.)

Further assume two implementations:

1. Fixed clock rate.
2. Variable clock rate, on a per-instruction basis.

Given an instruction mix: 24% loads, 12% stores, 44% R-format, 18% branches, 2% jumps, calculate the speedup of the variable clock rate machine.

Suppose we need to add a 15 ns. instruction that is used 5% (changing R-format percentage to 39%)?

1. A single cycle machine cannot take advantage of differences in instruction execution times.
2. In reality, we can't adjust the clock frequency dynamically.
3. What can we do?