

# Building a Datapath

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## 1 Administrivia

### Announcements

Homework due Wednesday. Exam Friday.

### Assignment

Read Section 5.3.

### From Last Time

Multiplication.

### Outline

1. Overview of the implementation.
2. Parts of the implementation.

### Coming Up

Merging the parts: a simple implementation.

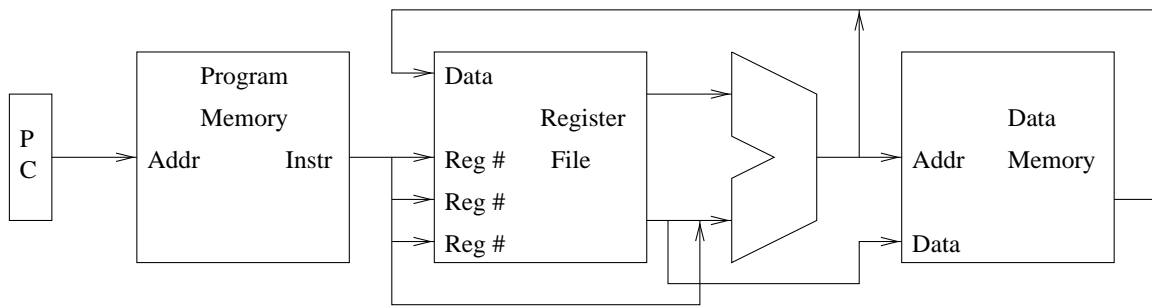
## 2 Overview of the MIPS Implementation

The general instruction cycle:

1. Instruction fetch.
2. Instruction decode.
3. Register fetch.
4. Operate.
5. Register store or memory operation.

How do the steps of the cycle fit each of the three instruction classes: arithmetic-logic, memory reference, branch?

A high level view of the implementation, in view of the instruction cycle:



1. Datapath only.
2. Is everything we need for our instructions here?

## 3 Building a Datapath

Strategy: Look at the major datapath components needed to execute each class of instructions.

Hardware needed:

1. Individual registers (PC).
2. Register file.
3. Memory (data memory).
4. ALU.
5. Sign extend, shift?

### **3.1 Instruction Fetch**

Common to all instruction formats.

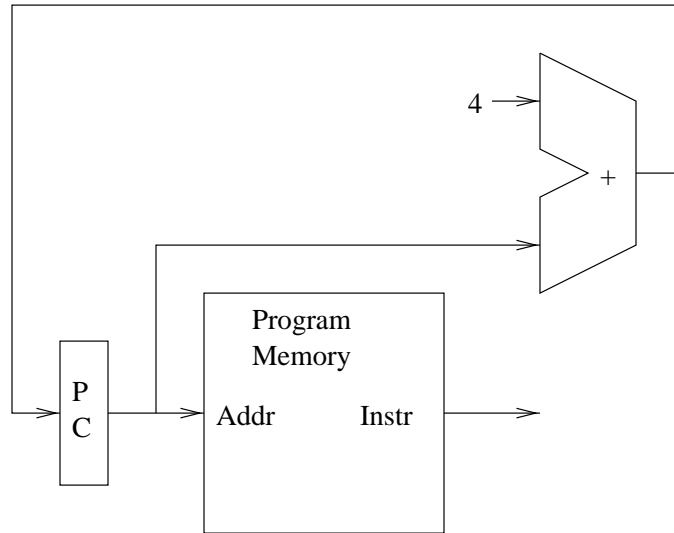
Requirements:

1. Store program.
2. Remember which instruction is to be executed next.
3. Fetch next instruction. (And store.)

Elements:

1. A register for the PC.
2. A memory for the program.
3. An adder to update the PC.

Organization:



The adder is a hardwired ALU.

### 3.2 R-Format

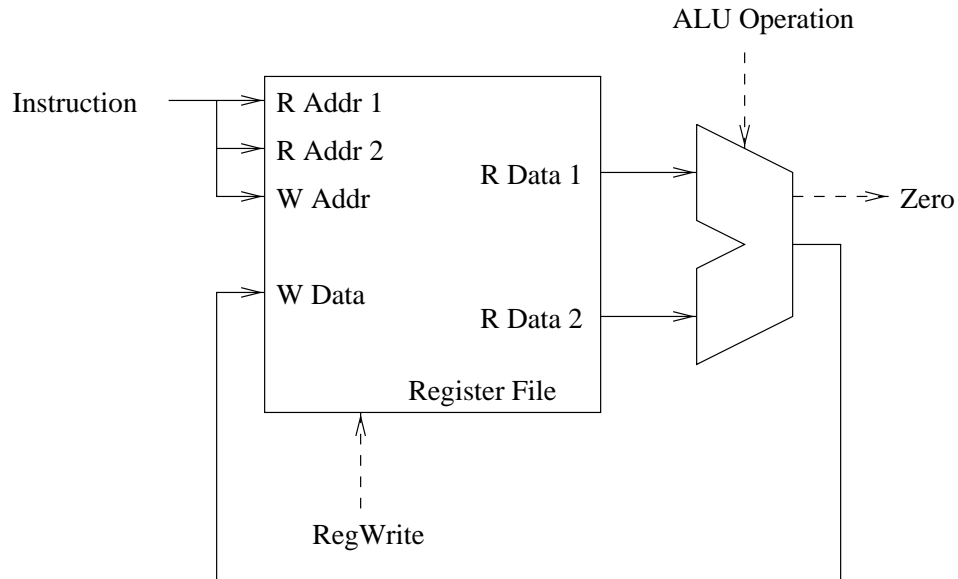
Requirements:

1. Fetch two register operands.
2. Operate.
3. Store result back into a register.

Elements:

1. A 32 word by 32 bit register file with two read ports and a write port (read B-25–B-26).
2. An ALU.

Organization:



Control signals: Write, ALU Control, Zero.

### 3.3 I-Format

Requirements:

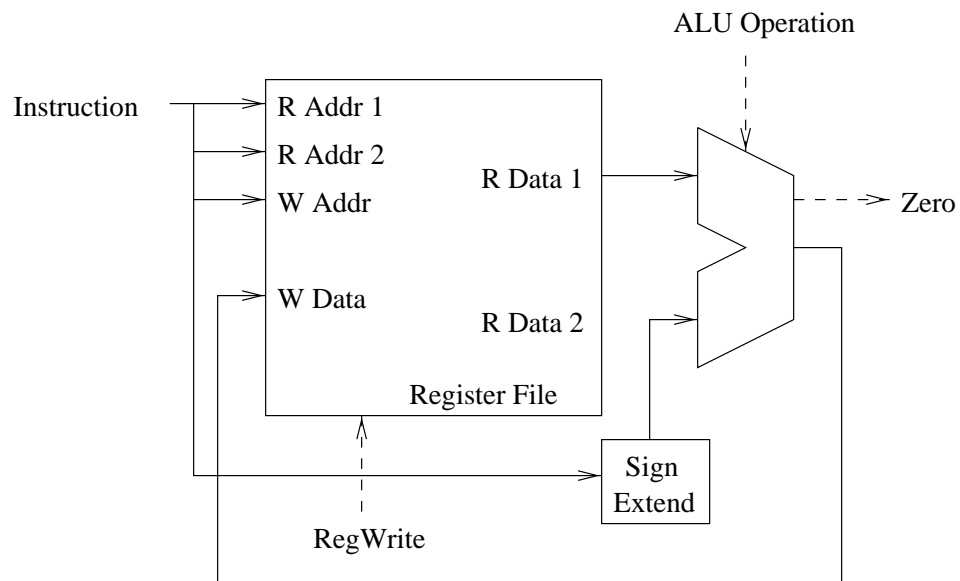
1. Immediate mode arithmetic-logic instructions:
  - (a) Replace one source register with sign-extended immediate value.
2. Memory reference instructions:
  - (a) Add base register and sign-extended offset.
  - (b) Transfer data
3. Branch instructions:
  - (a) Compare register values.
  - (b) Conditionally update PC with  $PC + 4 + \text{sign-extended, shifted offset}$ .

Elements: R-format elements plus:

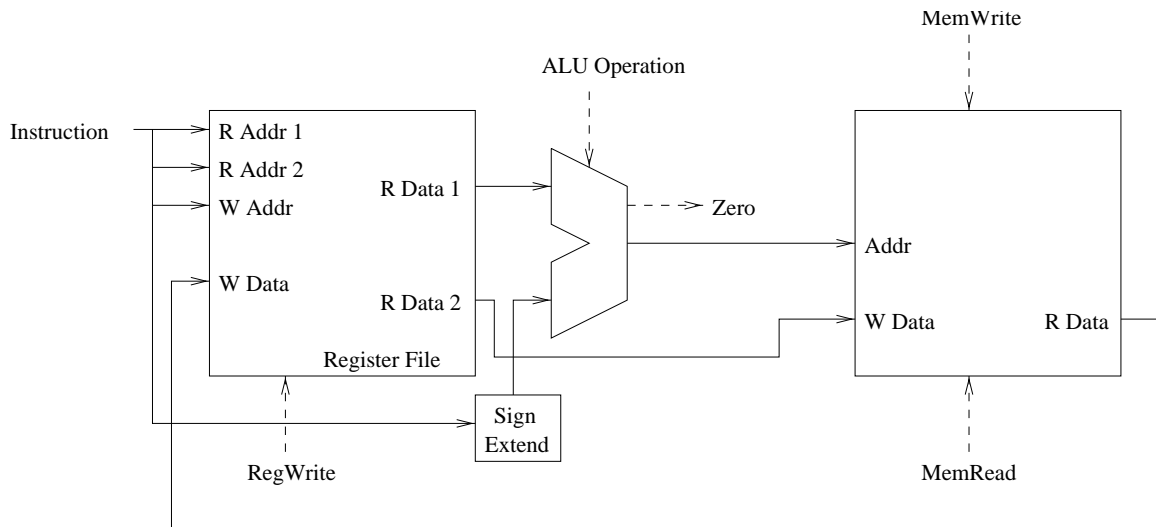
1. Substitution of a register source value with the immediate value.
2. A data memory.
3. A mechanism for loading a branch target address into the PC.

Organizations:

Immediate mode arithmetic-logic instructions:



Memory reference instructions:



Branch instructions:

