A Single-Cycle Implementation

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1 Administrivia

Announcements

Homework due Wednesday.

Assignment

Read 5.4.

From Last Time

Merging the datapaths.

Outline

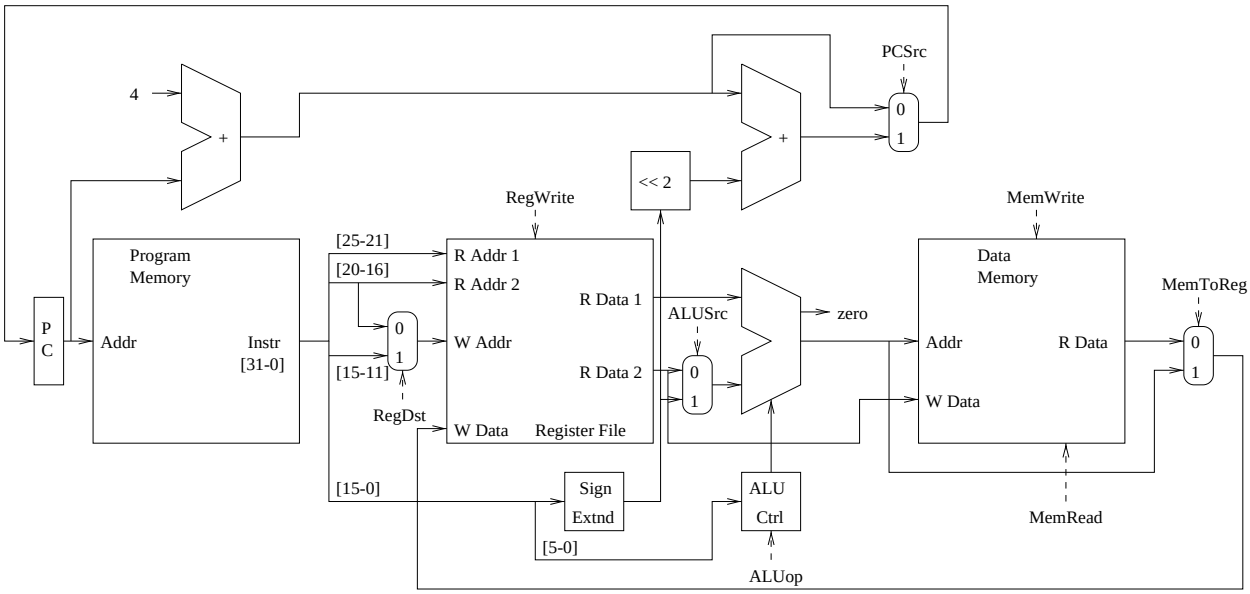
1. A simple implementation scheme.
2. The control unit.
3. Setting the control signals.

Coming Up

A multi-cycle implementation.

2 A Simple Implementation Scheme

The final, combined datapath:



Instructions implemented:

1. lw, sw.
2. beq.
3. add, sub, and, or, slt.

2.1 ALU Control

Recall ALU control inputs:

1. 000 — AND.
2. 001 — OR.
3. 010 — add.
4. 110 — subtract.
5. 111 — slt.

ALU op signals:

1. 00 — lw, sw.
2. 01 — beq.
3. 10 — R-format.

(Why did we choose this encoding?)

Funct field for R-format instructions:

1. 100000 — add.
2. 100010 — subtract.
3. 100100 — and.
4. 100101 — or.
5. 101010 — slt.

Note: no Funct field for other instructions.

Truth table for ALU control outputs?

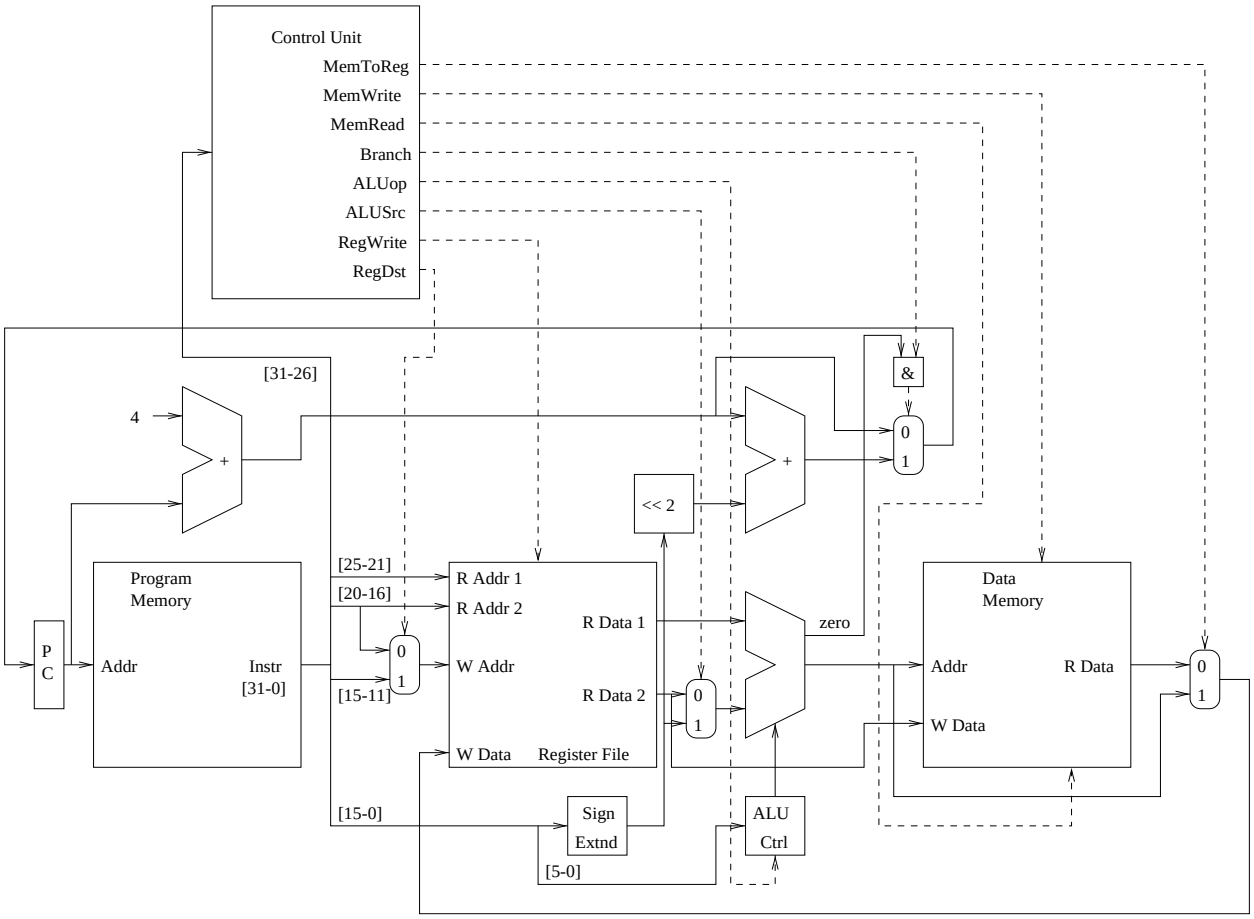
2.2 Control signals

1. RegDst — selects rt or rd field as write address.
2. RegWrite — write enable.
3. ALUsrc — selects rd2 or immediate data.
4. PCSrc — selects PC + 4 or branch target.
5. MemRead — read enable.
6. MemWrite — write enable.
7. MemToReg — selects ALU output or memory data to register file write data port.

3 The Control Unit

1. Is it combinational or sequential?
2. Why are its only inputs the opcode bits?

The control unit in place:



4 Setting the Control Signals

How should the control signals be set (0, 1, x) for each of the following?

1. R-format instructions.
2. lw.
3. sw.
4. beq.