Carry Lookahead Addition

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1 Administrivia

Announcements

Speaking of lookahead: HW II due 3/4, Exam I 3/8.

Assignment

Read 4.6.

From Last Time

MIPS ALU.

Outline

1. Preliminaries, "constant time addition."
2. Four-bit full carry lookahead adder.
3. Four-big Group carry lookahead unit.
4. Building large adders.

Coming Up

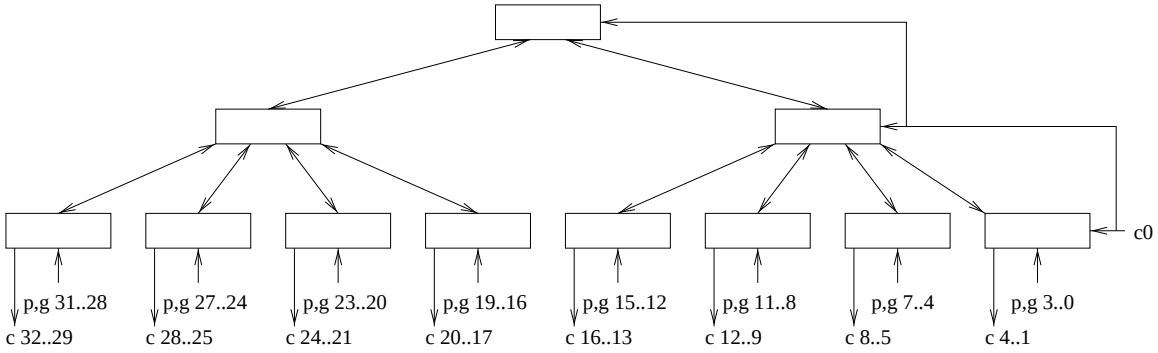
Multiplication.

2 Carry Lookahead Addition

1. Why bother with speeding up addition?
2. Divide and conquer approach to addition: $s_i = ps_i \oplus c_i$, where $ps_i = a_i \oplus b_i$.
3. Can we pre-compute the carries?
4. Carry generate: $g_i = a_i b_i$.
5. Carry propagate: $p_i = a_i + b_i$.
6. Illustration: look at p, g, and c for 11010101 and 01110011.
7. Some carry equations:
   (a) $c_1 = g_0 + p_0 c_0$
   (b) $c_2 = g_1 + p_1 c_1 = g_1 + p_1 g_0 + p_1 p_0 c_0$
   (c) $c_8 = g_7 + p_7 g_6 + p_7 p_6 g_5 + \cdots + p_7 p_6 p_5 p_4 p_3 p_2 p_1 p_0 c_0$
8. A bit of recursion:
   (a) Base case: c_0
   (b) Recursive step: $c_i = g_{i-1} + p_{i-1} c_{i-1}$
9. Why this isn't feasible. The Winograd lower bound.

2.1 Carry Lookahead: The Big Picture

Restricting the carry computation circuitry to a tree structure:

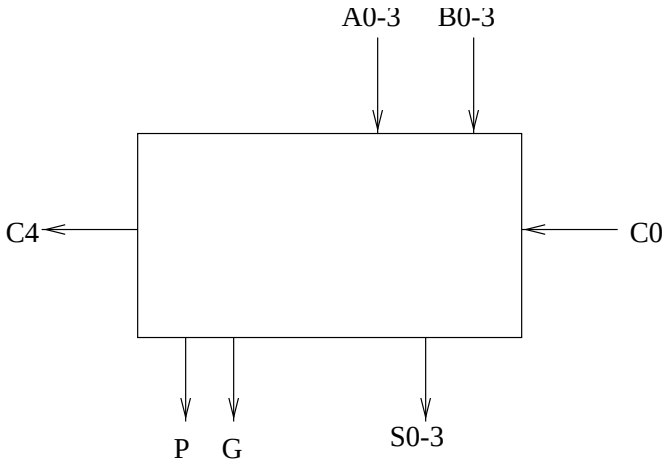


What does this buy us?

2.2 Four-Bit Carry Lookahead Adder

1. Design a four-bit full carry lookahead adder.

   Block diagram:



   Block generate, propagate.

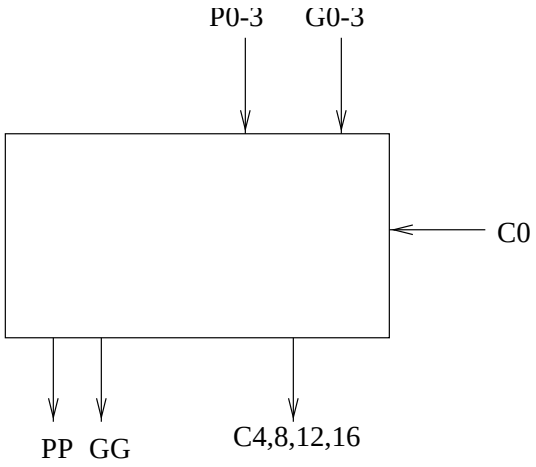
2. What is the fan-in?

3. What is the delay model from inputs to outputs?

2.3 4-Bit Group Carry Lookahead Unit

1. Design a 4-Group carry lookahead unit.

   Block diagram:



   Use of block generates, propagates.

2. What is the fan-in?

3. What is the delay model from inputs to outputs?

2.4 16-Bit Carry Lookahead Adders

Cascaded and full carry lookahead.

2.5 32-Bit Carry Lookahead Adders

Cascaded and full carry lookahead.