Macro Architectural Trends; IC Fabrication

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1 Administrivia

Announcements

Assignment

Read 2.1–2.6.

First homework will be posted later today.

From Last Time

Performance.

Outline

1.

Coming Up

2 Macro Architectural Trends

The power equation:

$$\text{Power} = \text{Capacitance} \times \text{Voltage}^2 \times \text{Clock Rate}$$

1. Capacitance: What is it, what contributes to it? Trends.
2. Voltage: Trends and limits.
3. Clock Rate: Trends.

"Sea change" from uniprocessing to multiprocessing:

1. Easy to increase uniprocessor performance if you can constantly overclock.
2. Explicit parallelism — the "third rail" of CA.
3. Explicit parallelism — we've been here before: supercomputers.
4. What's the future of this trend?

How did we get here?

1. The "Clock" wars.
2. Implicit parallelism — ILP:
   (a) Deep pipelining, branch prediction, speculative execution.
   (b) Trace caches.
   (c) Multiple issue.

    (d) Register renaming, out of order execution.

  The cost of high clock rates and all this complexity: power.

3. Heat dissipation in commodity microprocessors.

We've been here before: the CISC/RISC crossroads

1. CA was more art than science — few quantitative studies.
2. Trends:
    (a) Move software functionality into hardware — more and more HLL support.

        More "powerful" instructions are not always faster — the 11/780 `INDEX` instruction.

    (b) Historically, memory bandwidth had to be conserved.

        Achieved by:

        i. Dense, complex instruction sets.
        ii. Microcode techniques.
        iii. Feature creep.
3. Consequences:
    (a) Faster memory hierarchy.
    (b) "Irrational" implementations.
    (c) Increased design time.
    (d) Increased design errors.
4. Faster memory and VLSI technology broke the complexity trend.

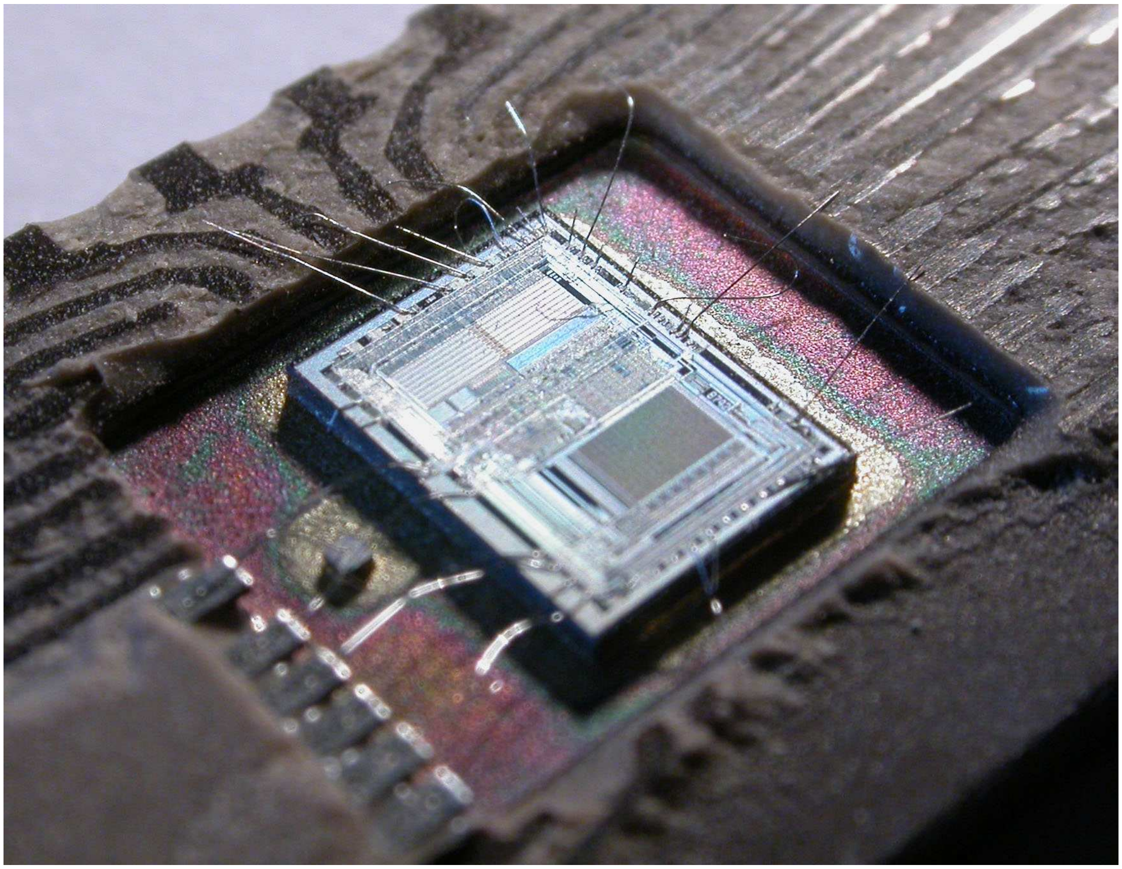
Moral of the story: re-evaluate your assumptions on a regular basis.

(Additional background: See “The Case for the Reduced Instruction Set Computer” on the web site.

3 IC Fabrication

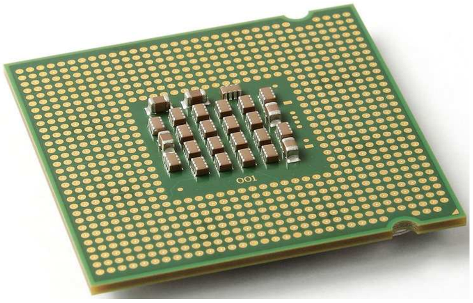
A little more background...

1. Die, package details.

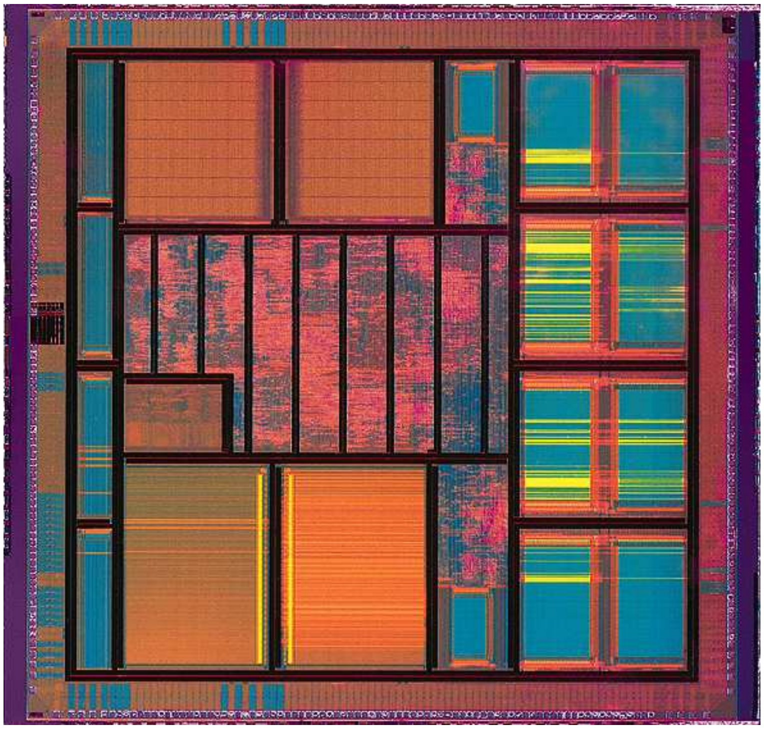


Core 2 Duo “Allendale” die size: 111 mm^2, 65 W, 775 pin LGA

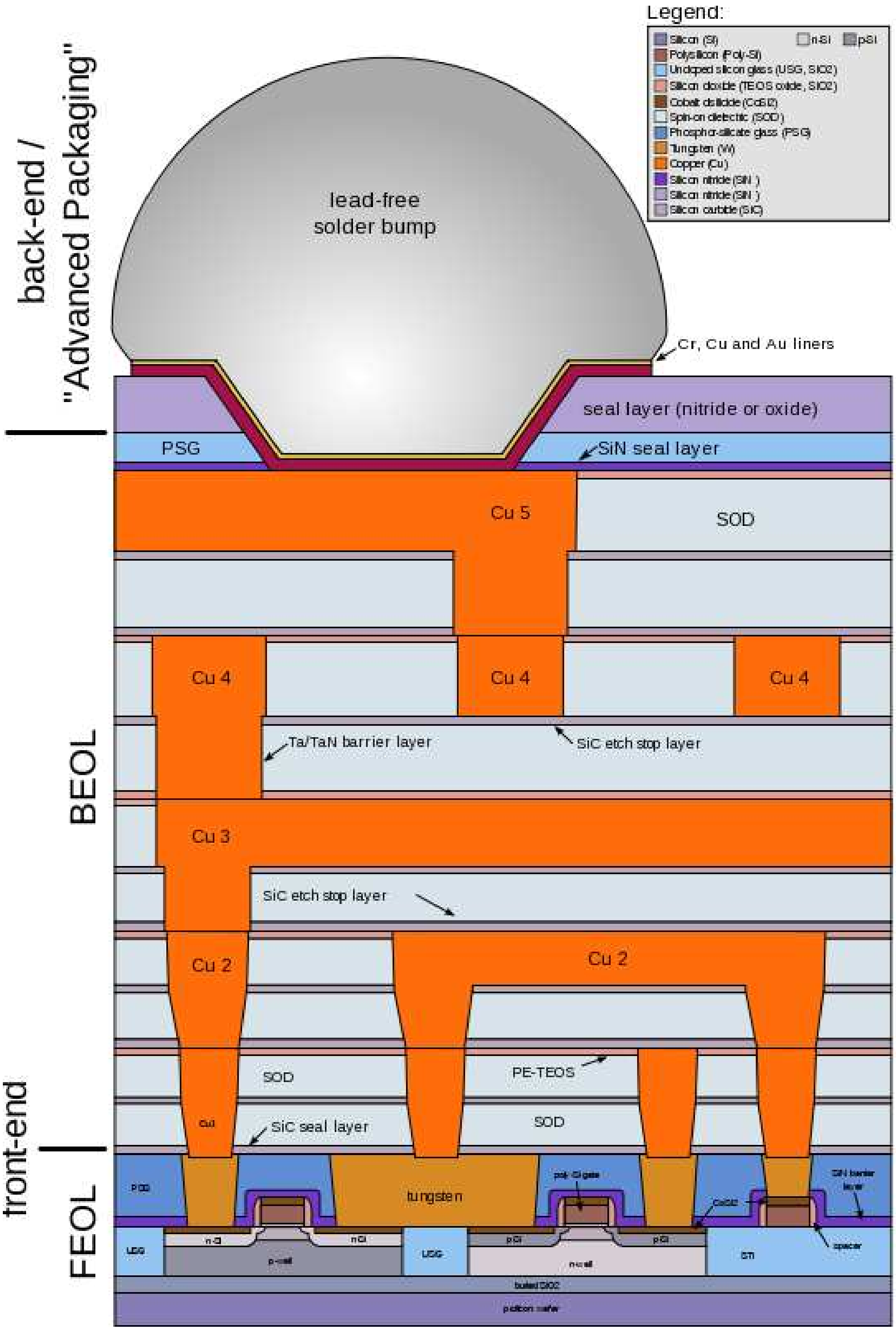

intel
Core™2 Duo



2. Die photomicrograph.



3. All features/layers are added in separate steps...



4. It all begins with design, either standard cell, schematic, VHDL, or hand-layout, resulting in a set of masks.