Instructor: Thomas P. Kelliher  
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Office hours: MWF 10:30–11:20am. Th 1:00–3:00pm. Other times by appointment.

Class: Hoffman 149  
MWF 1:30–2:20pm  
Three credits.  

Objectives:  
• Understand how logic gates are used to design and build combinational and sequential logic.  
• Implement some hardware designs using the Xilinx toolset and Xilinx FPGAs.


Grading: Grade Distribution  
A = [92%–100%], A- = [90%–92%), B+ = [88%–90%), B = [82%–88%), B- = [80%–82%), etc. Grades are “one point rounded.”

Course Point Distribution  
There are tentatively 700 total points for the course:

1. Assignments. There will be approximately six written assignments. Each assignment will be worth 50 points. 10% of the maximum grade will be deducted per day from late assignments (the weekend counts as one day). Assignments over three days late will not be accepted.

2. Semester exams. There will be two exams, on the following dates: Oct. 10 and Nov. 14. Each will be worth 100 points.

3. Final. There will be a cumulative final, scheduled by SAS. The final is worth 200 points.

Current grades (password protected) may be viewed on the class home page.
Course Handouts: Course handouts will be made available once in class. After that, they may be obtained from the class home page.

Attendance: Attendance of classes is expected. It is your responsibility to catch up on missed class work.

Electronic Communication: From time-to-time, I will need to send e-mail messages to the class. These messages will be addressed to your official Goucher e-mail addresses. You are responsible for checking your e-mail on a timely basis.

Distractions: Cell phones must be turned off or set to “silent” during class. If you must enter late, do so as unobtrusively as possible. Likewise if you must leave early. Please use mental telepathy if you must hold a personal conference during class. I have ways of making you not talk!

Integrity: Academic dishonesty will not be tolerated. We are all bound by the Academic Honor Code.