Curriculum Vitae

Thomas P. Kelliher

Department of Mathematics and
Computer Science
Goucher College
1021 Dulaney Valley Rd.
Baltimore, MD 21204

Phone: (410) 337-6189
Fax: (410) 337-6408
kelliher@goucher.edu
http://phoenix.goucher.edu/~kelliher/

Education

1993 Ph.D., Computer Science, The Pennsylvania State University, University Park, PA.

Computer Science, Villanova University, Villanova, PA. Graduate course work, 1985–1986 academic year.

1983 B.E.S., Electrical Engineering and Computer Science, The Johns Hopkins University, Baltimore, MD.

Employment History

9/02–present Associate Professor, Mathematics and Computer Science, Goucher College, Baltimore, MD.

7/03–6/06 Department Chair, Mathematics and Computer Science, Goucher College, Baltimore, MD.

8/97–8/02 Assistant Professor, Mathematics and Computer Science, Goucher College, Baltimore, MD.

8/93–7/97 Assistant Professor, Mathematics and Computer Science, Westminster College, New Wilmington, PA.

8/92–8/93 Postdoctoral Scholar, Computer Science, The Pennsylvania State University, University Park, PA.

8/86–8/92 Research and Teaching Assistant, The Pennsylvania State University, University Park, PA.

6/83–7/86 Engineer, Burroughs Corporation, Tredyffrin, PA. Received Achievement Award.

5/85–7/86 A12 project. Lead designer of the memory controller. Development and debug.

6/83–8/85 A15 project. Design, development, and debug of the A15's memory controller.

Academic Activities

Courses Taught: Functions & Graphs, Computers & Society, Internet Cluster Course (Computer Science and Psychology), Computer Literacy, Fortran Programming for Engineers, Discrete Mathematics I, Introduction to Computer Science, Principles of Computer

Science I, Principles of Computer Science II, Data Structures, Software Tools, Computer Organization, Computer Architecture, Operating Systems, Distributed Systems, Computer Networks, Software Engineering, Database Systems, Computer Graphics, Parallel Algorithms, Computing Security.

Independent Studies Supervised: Principles of Programming Languages, Perl Programming for the World Wide Web, Operating Systems, Distributed Systems, Computer Graphics, Database Design for the Soda Machine Project, Computer Organization, Computing Security.

Student Coaching: ACM Programming Contest, Johns Hopkins University, Nov. 2000–2002, Nov. 2004–2008.

Supervision: Graduate students involved in MGAP research at Penn State, summers, 1994–1997. Graduate students involved in advanced multimedia processor architectures research, 6/97–8/04.

Ph.D. Committee Membership:

1/94 M. Shashi, "Intelligent Legal Assistant for Adjudication," Computer Science and Engineering, Andhra University, India.

8/95 R. Bajwa, "Reconfigurable Architectures," Computer Science and Engineering, Penn State.

5/96 C. Nagendra, "Power, Delay, and Area Tradeoffs in VLSI Arithmetic Circuits," Computer Science and Engineering, Penn State.

8/00 B. Bishop, "Issues in High Performance Multimedia" Computer Science and Engineering, Penn State.

Undergraduate Research Supervision:

6/02–8/02 S. Abbott, Floating Point Iterative System Architectures, University of Georgia. Funded by Goucher College.

6/99–8/99 A. Shao, SPARTA Project, Penn State. Funded by Goucher College.

1/99– A. Badik, et al., The Soda Machine Project: COLA (Coke On-Line Appliance). Funded by Goucher College.

10/94–5/95 T. Chihaya, "A World Wide Web Server for Westminster College," Westminster College.

8/95–5/96 K. Arner, continued development of the Westminster College WWW server. Westminster College.

Grants

T. P. Kelliher, Crosby Grant from Goucher College in support of a file server for storing virtual machine images, $1,000, December 2008.

T. P. Kelliher, donation from VMware Corporation of VMware Workstation software, $1,277, October 2008.

T. P. Kelliher, donation from Xilinx Corporation of five XESS XSA-50 FPGA Prototyping boards, $750, September 2004.

T. P. Kelliher, donation from SSH Communications Corporation of SSH Secure Shell for Workstations for Windows software, $8,700, July 2002.

B. Bishop and T. P. Kelliher, "Floating Point Intensive Reconfigurable Computer for Interactive Applications." MOSIS Educational Program, $22,400, July 2001.

T. P. Kelliher, donation from Xilinx Corporation of Foundations Elite FPGA design suite, four licenses, and four XESS XS40-010XL FPGA Prototyping boards, $2,581, July 2001.

S. K. Webster, B. B. Cindric, T. P. Kelliher, and A. G. Gittis, "Neural, Social and Electronic Networks: A Cluster Course Approach," NSF DUE, Undergraduate Instrumentation and Lab Improvement, 9651206, $17,232.00, June 1996.

Research Activities

Interest Areas: Computer Architecture (3D graphics, multimedia processors, low-power processors, parallel architectures, application specific systems, high performance memory systems, computer arithmetic), distributed systems (networked appliances, authentication, security, encryption), and VLSI systems.

5/01– Floating Point Intensive Reconfigurable Computer for Interactive Applications.

1/98–8/00 SPARTA: Simulation of Physics in a Realtime Architecture.

6/97–8/00 Issues in multimedia processor architectures.

10/93–5/97 The Micro-Grained Array Processor II.

5/92–10/93 The Micro-Grained Array Processor I.

8/89–5/92 The Arithmetic Cube II.

Professional Activities

Grant proposal reviewer, National Science Foundation, September 2005.

Organizer, *Peace and the Internet Conference*, Goucher College, March 2001.

Memberships: ACM (SIGARCH, SIGCSE), IEEE, IEEE Computer Society, CPSR, AAUP.

Journal and Refereed Conference Publications

S. Yardi, B. Bishop, T. P. Kelliher, "HELLAS: A Specialized Architecture for Interactive Deformable Object Modeling," *ACM Southeast Conference*, Melbourne, FL, March 10-12, 2006.

S. Yardi, B. Bishop, and T. P. Kelliher, "An Analysis of Interactive Deformable Solid Object Modeling." *2005 International Multiconference in Computer Science and Computer Engineering*, World Academy of Science. June 27-30, 2005, pp. 95-99.

B. Bishop and T. P. Kelliher, "Specialized Hardware for Deformable Object Modeling," *IEEE Transactions on Circuits and Systems for Video Technology*. 13(11):1074–1079. Nov. 2003.

B. Bishop and T. P. Kelliher, "Reconfigurable Computing for Floating Point Intensive Iterative Applications." *10th ACM Symp. on Field-Programmable Gate Arrays*. Feb. 2001, Monterey, CA.

E. S. Gayles, T. P. Kelliher, R. M. Owens, and M. J. Irwin, "The Design of the MGAP-2: A Micro-Grained Massively Parallel Array." *IEEE Trans. on VLSI Sys*. 8(6):709–716. Dec. 2000.

B. Bishop and T. P. Kelliher, "Hardware Acceleration for Physical Modeling of Deformable Objects." *ACM SIGGRAPH Conference* (technical sketch), Aug. 2001, Los Angeles, CA.

B. Bishop, T. P. Kelliher, and M. J. Irwin, "A Detailed Analysis of MediaBench." *1999 IEEE Workshop on Signal Processing Systems*. Taipei, Taiwan. November 1999.

B. Bishop, T. P. Kelliher and M. J. Irwin, "Hardware/Software Co-Design for Real-Time Physical Modeling." *2000 IEEE International Conference on Multimedia and Expo*, New York, NY, Aug. 2000.

B. Bishop, T. P. Kelliher and M. J. Irwin, "SPARTA: Simulation of Physics on A Real-Time Architecture." *10th Great Lakes Symposium on VLSI*, Evanston, IL, March 2000.

S. K. Webster and T. P. Kelliher, "Intro through Internet Psychology." *Resources in Education*, ERIC CASS, CG029218.

B. Bishop, T. P. Kelliher, R. M. Owens, and M. J. Irwin, "Aggressive Dynamic Execution of Decoded Traces." *Journal of VLSI Signal Processing*. 22(1), Aug. 1999.

T. P. Kelliher, J. Zimmerman, and S. K. Webster, "Cyberfluency in the 21st Century: Vive Le Cyberspace." *1999 ASCUE Annual Summer Conference*. Myrtle Beach, SC. June, 1999.

B. Bishop, T. P. Kelliher, and M. J. Irwin, "The Design of a Register Renaming Unit." In Proc. 9th Great Lakes Symposium on VLSI, pp.34–37, Ann Arbor, MI, March 4–6 1999.

B. Bishop, T. P. Kelliher, R. M. Owens and M. J. Irwin, "Re-Evaluating MPEG Motion Compensation Search Criteria." *1998 IEEE Workshop on Signal Processing Systems*. Cambridge, MA. Oct. 1998.

S. K. Webster and T. P. Kelliher, "Intro through Internet Psychology." Poster, The 106th Annual Meeting of the American Psychological Association, San Francisco, CA, Aug. 14–18 1998.

T. P. Kelliher and S. K. Webster, "Beyond Computer Literacy: Vive Le Cyberspace." Presented at *EDUCOM '97*. Minneapolis, MN. Nov. 1997.

T. P. Kelliher, B. J. Bishop, Y. Zhang, E. S. Gayles, R. M. Owens, M. J. Irwin, "The MGAP-2: Demonstration of a Massively Parallel Micro-Grained Array Processor." Research Exhibit, *Supercomputing '96*.

T. P. Kelliher, R. M. Owens, M. J. Irwin, "The MGAP-2 Processor Array and System." *Supercomputing '96*.

R. S. Bajwa, R. M. Owens, and T. P. Kelliher, "Simultaneous Speech Segmentation and Phoneme Recognition Using Dynamic Programming." *ICASSP '96.*

C. Nagendra, P. Keltcher, R. S. Bajwa, H. N. Kim, M. Borah, E. S. Gayles, K. P. Acken, H. Mehta, T. P. Kelliher, R. M. Owens, and M. J. Irwin, "The MGAP-2: A Fine-Grain High-Performance Co-Processor." *Supercomputing '95*.

T. P. Kelliher, E. S. Gayles, R. M. Owens, and M. J. Irwin, "The MGAP-2: An Advanced, Massively Parallel VLSI Signal Processor." *ICASSP '95*, May 1995.

F. Zhou, T. P. Kelliher, R. M. Owens, and M. J. Irwin, "Introducing MGAP-2." In *Frontiers '95*, pp. 281–288, Feb. 1995.

R. M. Owens, T. P. Kelliher, M. J. Irwin, M. Vishwanath, R. S. Bajwa, and W.-L. Yang, "The Design and Implementation of the Arithmetic Cube II, A VLSI Signal Processing System." *IEEE Transactions on VLSI Systems*, Pages 491–502, Dec. 1993.

C. Nagendra, R. Bajwa, P. Keltcher, T. Kelliher, R. Owens, and M. J. Irwin, "The Micro-Grain Array Processor." *1993 IEEE Winter VLSI Workshop*.

R. M. Owens, T. P. Kelliher, and M. J. Irwin, "Building High Performance Signal Processors Cheaply and Quickly." *1993 IEEE Workshop on VLSI Signal Processing*, Oct. 1993.

T. P. Kelliher, "The Arithmetic Cube II and Memory Based Architecture for Data Structure Manipulation." Ph.D. Thesis, The Pennsylvania State University, May 1993.

T. P. Kelliher and M. J. Irwin, "A Systolic VLSI Architecture for Multi-Dimensional Transforms." *ICASSP 1993*.

R. M. Owens, M. J. Irwin, T. P. Kelliher, M. Vishwanath, and R. S. Bajwa, "Building a High-Performance Signal Processing Architecture: Arithmetic Cube II." In *GOMAC 1992*, pages 97–100, November 1992.

T. P. Kelliher, R. M. Owens, M. J. Irwin, and T.-T. Hwang, "ELM — A Fast Addition Algorithm Discovered by a Program." *IEEE Trans. on Comps.*, pages 1181–1184, September 1992.

R. M. Owens, M. J. Irwin, T. P. Kelliher, M. Vishwanath, and R. S. Bajwa, "Implementing a Family of High Performance, Micrograined Architectures." In *Intl. Conf. Application-Specific Array Processors 1992*, pages 191–205, August 1992.

M. J. Irwin, R. M. Owens, T. P. Kelliher, K.-K. Leung, and M. Vishwanath, "The Arithmetic Cube II: A Second Generation VLSI DSP Processor." In *ICASSP*, pages 1125–1128, May 1991.

T. P. Kelliher, C.-M. Wu, R. M. Owens, and M. J. Irwin, "The Design of the Arithmetic Cube II." In *VLSI Signal Processing IV*, pages 95–105, Nov. 1990.

R. M. Owens, M. J. Irwin, T. P. Kelliher, and C.-M. J. Wu, "The Arithmetic Cube: A Highly Parallel VLSI DSP Architecture." In *Proc. IFIP Workshop on Parallel Arch. on Silicon:*

From Systolic Arrays to Neural Nets, France, Dec. 1989. Institut National Polytechnique de Grenoble.

Conference Presentations

B. Tutinas and T. P. Kelliher, "Just in Time Teaching," CTLT *Active Learning Conference*, Goucher College, MD. May 2004.

T. P. Kelliher and J. Zimmerman, "The Internet Influencing Society Influencing the Internet Influ..." *Peace and the Internet*, Goucher College, MD. March 2001.

J. Zimmerman and T. P. Kelliher, "A Computer Scientist's Virtual Toolbox." *Collegetown Network Conference: Best Practices in Teaching with Technology*. Goucher College, MD. March 2001.

Invited Talks

"The New Revolution: Information Technology." Quest Program, Westminster College, New Wilmington, PA, May, 1996.

"Computing: What Now? What Next?" Faculty Forum, Westminster College, New Wilmington, PA, Oct, 1995.

"Introducing MGAP-2." Department of Computer Science and Engineering, Penn State, University Park, PA, January, 1995.

"In Search of a Teraop." Department of Mathematics and Computer Science, Westminster College, New Wilmington, PA, February, 1995.

"The Silicon Shell Game: Constant Time Computer Addition." Department of Mathematics and Computer Science, Westminster College, New Wilmington, PA, February, 1994.

Service

7/08–present Chair of the Faculty.

7/08–present Budget Committee of the Goucher College Board of Trustees.

9/08–5/09 Financial Exigency ad hoc committee.

7/07–4/09 Co-Chair, Middle States Self Study Steering Committee.

4/06–11/06 Provost Search Committee.

1/06-6/06 Lectures and Fellowships Committee.

9/04–present Fair Use Committee.

1/05–5/05 Consensual Relationship Review Task Force.

9/04–6/08 Faculty parliamentarian.

9/03–5/08 MaCS/PME Club adviser.

9/02–5/03 Strategic Planning Sub-Committee on Internationalism and Interculturalism.

9/02–5/04 Task Force on Intellectual Property Policy.

9/02–5/03 Task Force on Portfolios.

9/01–6/04 Curriculum Committee, secretary.

9/01–5/02 Faculty Executive Council.

9/00–5/02 Trustee Task Force on Communications and Technology.

9/00–present ITAG. Secretary from 1/01–5/02.

3/01 Member, Presidential Scholar Selection Committee.

6/98–present Pre-major adviser, Goucher College

9/98–8/03 Treasurer, Faculty Affairs Committee, Goucher College

9/97–8/99 Librarian, Math & CS Department

9/97–present System administration and computing infrastructure support, Math & CS Department, Goucher College

10/96–1/97 Member, Taskforce for recommending the public computing laboratories' operating system, Westminster College

1/95–5/96 Member, Learning Applications Team, Westminster College.

8/94–7/97 Director and Administrator, Department of Mathematics and Computer Science Unix laboratory, Westminster College.

9/93–7/97 Faculty Adviser, UPE Computer Science Honorary, Westminster College.