

Xilinx Test Programs

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This documents shows the pin constraints for the 2's complement and electronic lock problems so that you can confirm the Pinout Reports. In addition, one of the Synthesize process properties must be changed for the 2's complement problem. This document also describes how to perform FPGA testing for these two problems.

1 Performing FPGA Testing

2's Complement Problem

1. Synthesize process property change:
 - (a) Open the Project menu, choose Cleanup Project Files and click the OK button.
 - (b) Right-click the Synthesize tool and select Process Properties. Select the HDL Options category and change the FSM Encoding Algorithm to None.
 - (c) Run the Synthesize, Implement Design, and Generate Programming File tools.
2. Download the test driver program from the class Web site. The program is named `comp2.exe`. Source code is available for your inspection.
3. Configure the FPGA board with a bitstream. Then, open a command line window. You can do this by opening the Start menu, typing `cmd` in the search field, and pressing Enter.
4. Using `cd` in the command line window, navigate to the folder containing the executable test program. Type its name and press Enter. It will begin to run. It's operation should be self-explanatory.
5. Test your circuit with several input values. Report the values tested and the results.

Electronic Lock Problem

1. The pin constraints for this problem are set so that T is BTN3, K is BTN2, Lock is BTN1, and Unlock is BTN0. Locked is LD2, Unlocked is LD1, and IgnoringInputs is LD0.
2. Test several input sequences. Report each test sequence and the result.

2 Pin Constraints for 2's Complement Problem

Signal	Location
mclk	B8
pdb(7)	R10
pdb(6)	P10
pdb(5)	R11
pdb(4)	N11
pdb(3)	T12
pdb(2)	P13
pdb(1)	R13
pdb(0)	R14
astb	V14
dstb	U14
pwr	V16
pwait	N9
rgan(3)	F15
rgan(2)	C18
rgan(1)	H17
rgan(0)	F17

3 Pin Constraints for the Electronic Lock Problem

Signal	Location
clk	B8
T	H13
K	E18
Lock	D18
Unlock	B18
Locked	K15
Unlocked	J15
IgnoringInputs	J14