# Homework VII

Tom Kelliher, CS 240

25 points, recommended due date of April 27

The final deadline for this assignment is 12:00 pm on Friday, May 4.

1. Design a serial 2's complementer circuit. A 2's complement number of unknown length is given as input to the circuit, least significant bit first, on input `X`. When a given bit is input, the corresponding output bit is to appear on output `Z`, on the same clock cycle (Mealy machine). A second input, `RESET`, is used to reset the circuit to its initial state on the next rising clock edge (synchronous reset) so that the circuit is prepared to receive the next 2's complement number beginning with the next clock cycle. `RESET` is active-high.

   (a) Determine the state diagram for this sequential circuit.

   (b) Make state assignments and determine the state table for this circuit.

   (c) Implement your design in VHDL. Then, download your design to one of the FPGA boards, run my test program to test your circuit, and report the result.

2. Tom's super-secret chocolate stash is guarded with an electronic lock that has four push-buttons: `T`, `K`, `Lock`, and `Unlock`. If the lock is in the locked state, the following sequence of button pushes will unlock the lock: `T K K T Unlock`. Pressing the `Lock` button will lock the lock and also cause it to forget any previously-entered button pushes. Should a button push sequence other than the above sequence be entered, the lock should ignore further inputs until the `Lock` button is pushed. The lock has three outputs: `Locked`, `Unlocked`, and `IgnoringInputs`.

   (a) Determine the state diagram for this sequential circuit.

   (b) Make state assignments and determine the state table for this circuit.

   (c) Implement your design in VHDL. Then, download your design to one of the FPGA boards, test your circuit, and report the result.

For both problems, submit **hardcopy** of your state diagram, state table, VHDL source code, and the report of your test result. The test result report should be written in literate English. Electronic assignment submissions will not be accepted.

I won't make the Xilinx boards available until you're ready to use them. Please give me advance notice of when you plan to begin using the boards.