

Homework V

Tom Kelliher, CS 240

25 points, due Mar. 28

Using structural VHDL, design, synthesize, and simulate the four-bit comparator from problem 4-11 in the textbook. Your solution should consist of two VHDL entities. The first entity should be the one-bit comparator you designed in Homework IV. This entity should use components from `lcdf_vhdl.func_prims.all` and use this entity statement as its starting point:

```
entity COMP1 is
  port(a, b, xi : in  std_logic;
        xo      : out std_logic);
end COMP1;
```

Synthesize and simulate this entity.

The second entity should be the four-bit comparator you designed by cascading four of the one-bit comparators. This comparator should use `COMP1` as a component, instantiated four times. Use the following entity statement for this comparator:

```
entity COMP4 is
  port(a, b, : in  std_logic_vector(3 downto 0);
        x    : out std_logic);
end COMP4;
```

Synthesize and simulate this entity.

The `COMP1` entity should be tested exhaustively. The `COMP4` entity should be tested fully enough to convince someone other than yourself that it is functioning correctly. It should *not* be tested exhaustively. Include a paragraph or two of commentary explaining what test cases you selected for the `COMP4` entity, why you selected them, and how they demonstrate the correct functioning of the `COMP4` entity.

Turn-in your VHDL source files (module files and test bench files), your test waveforms from ISim, and your test cases commentary.