Memory: ROM and RAM

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1 Administrivia

Announcements

Lab day Wednesday; I won't be around this weekend or Monday.

Assignment

From Last Time

Counters

Outline

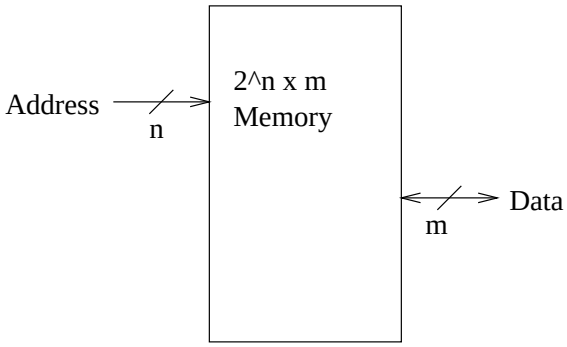
1. Introduction.
2. ROM, FLASH.
3. RAM.

Coming Up

Lab day.

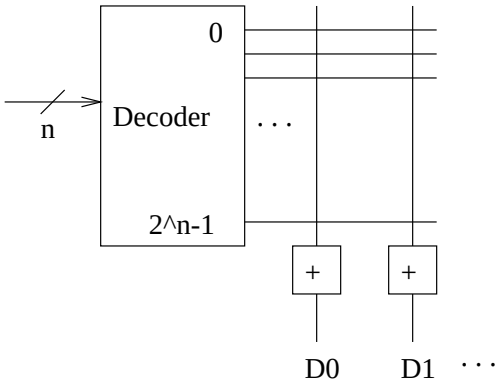
2 Introduction

1. What is memory?
2. Volatile vs. non-volatile.
3. RAM characteristics: speed, density, power.
4. Memory hierarchy: registers, cache, main memory, etc.
5. General structure:



3 ROM

1. Technologies: PROM, EPROM (UV), EEPROM, EAPROM, FLASH.
2. Where do you find ROM in a PC?
3. Structure of a ROM:



Minterms, fusible links.

4. Usage: program storage, generation of combinational functions.

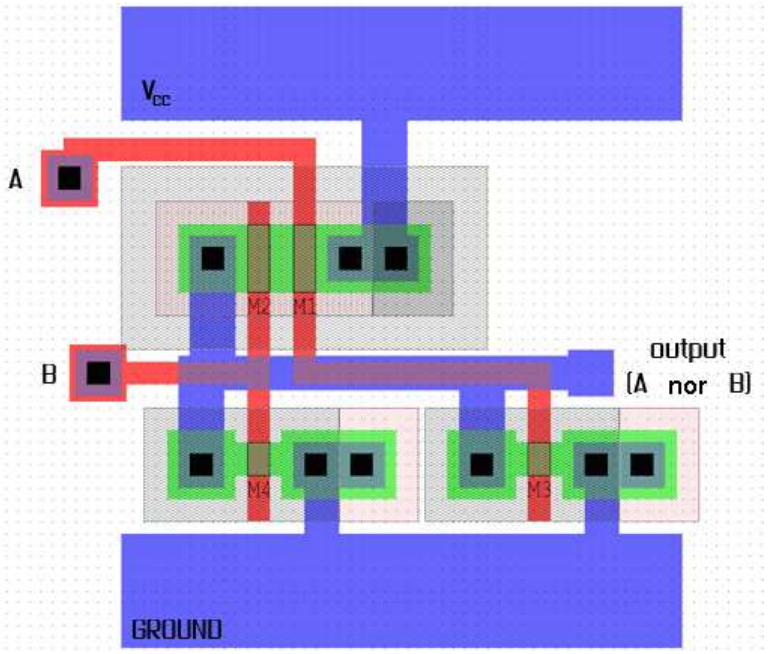
   How do you use for combinational functions?

3.1 FLASH

1. A specific type of EEPROM.
2. Erasure sets all the bits (to 1).

   Programming/writing resets a bit (to 0).
3. Two types:
   (a) NOR:
      i. Cells connected in parallel to bit lines. Allows random access.

         Similar to pull-down plane in a NOR gate, hence the name.



      ii. Long erase and write times.

iii. Allows random access to any memory location.

"Drop-in" replacement for ROM (system BIOS, other firmware).

iv. Sustains 10^5 erase cycles.

(b) NAND:

i. Cells connected in series to bit lines. Prohibits random access.

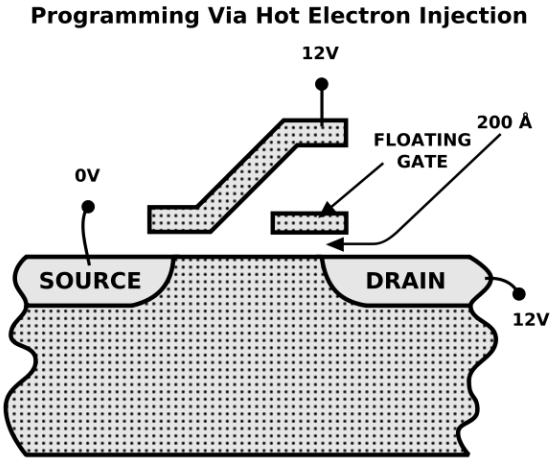
ii. Faster erase and write times. Denser.

iii. Block-oriented access. Suitable for secondary storage.

Block may consist of 64 pages of 2 KB each. Writes can be done on a per page basis; erases on a per block basis.

iv. Sustains 10^6 erase cycles.

4. Programming NOR FLASH



(a) Cell resembles standard MOSFET, but there is a second, insulated gate — the "floating gate," which is completely insulated by the oxide layer.

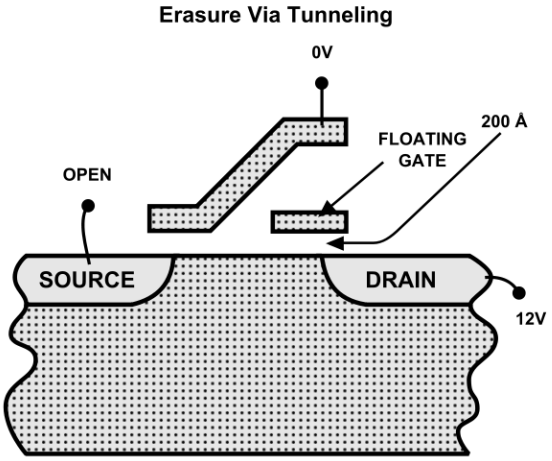
(b) To program, an elevated voltage is applied to gate and drain. Channel conducts.

(c) Elevated voltage created by a charge pump.

(d) Source/drain current high enough to allow some high-energy electrons to jump to the FG, charging it. This charge is essentially permanent.

(e) Charge on FG modifies the threshold voltage, essentially forcing the transistor into an always open state (non-conducting), storing a 0.

5. Erasing NOR FLASH



(a) Apply large negative voltage from drain to gate.

(b) Electrons on FG are pulled to drain via quantum tunnelling.

(c) Threshold voltage restored, allowing transistor to once again conduct, storing a 1.

(d) Cells are erased in blocks.

6. Memory wear, bad block detection and management, wear levelling.

Remap blocks around bad spots, or to level erasure effects. (Per block erasure counters needed).

Checksums used to detect and correct block failures.

4 RAM

1. Additional inputs: !Enable, Read/!Write

2. Static RAM: latches, inverter pair.

   Used for caches. Fast. Not dense. High power.

3. Dynamic RAM: stored charge on a capacitor.

   (a) Leakage, refresh.

   (b) Used for main memory. Slow. Dense. Low power.

   (c) Sizes. I/O pin limitations. Solutions: one bit wide, address multiplexing. 2-D structure.

   (d) Additional inputs: RAS, CAS.

4. Read/Write sequences.

   Write strobe with respect to the clock signal. Importance of address bus settling before write asserts.