Xilinx Tools Lab

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1 Administrivia

Announcements

Assignment

Read 5.1–2.

From Last Time

Dataflow, hierarchical, behavioral VHDL design styles.

Outline

1. Introduction.
2. Lab.

Coming Up

Introduction to sequential circuits. Latches.

2 Introduction

For `EXOR3` circuit demonstrate:

1. Library tab and set-up.
2. Syntax checking.
3. Synthesis.
4. Testbench waveform.
5. Behavioral simulation and zooming.

3 Lab

1. Implement and simulate `EXOR3`.

   The source and library VHDL are on the class Web site. There are syntax errors in the source VHDL which you'll need to find and fix.

2. Implement:

   (a) A 4-1 mux.

   (b) A hierarchical four-bit adder, using the fa component (see class Web site).

   (c) An eight-input priority encoder. This circuit has eight one bit inputs, one three bit output (the encoded value of the prioritized input), and a one bit valid output.

   Hint, try this construct:

```
o <= "111" when i(7) = '1' else
     "110" when i(6) = '1' else
     ...
     "000";
```

   (Avoid don't cares.)