Homework IV

Tom Kelliher, CS 240

50 points, due Mar. 12

1. (10 pts.) 3-40. Use only the logic building blocks mentioned in the problem.

2. (10 pts.) 4-11. Hint: This is a circuit with eight inputs. You probably *dont't* want to construct the truth table for this circuit. Instead, consider a modular divide-and-conquer approach, similar to how one uses divide-and-conquer when designing an n-bit adder from n one-bit full adders. Your one-bit module will have three single-bit inputs and one single-bit output; you'll have to decide what the inputs and output represent. You will need to carefully consider whether the module outputs propagate from the least significant bit toward the most significant bit (a la addition) or in the opposite direction.

3. (20 pts.) Design three 64-bit adders, including figures showing the connections between components:

   (a) A ripple carry adder using 64 one-bit full adders.

   (b) A partial carry-lookahead adder, using 16 4-bit carry-lookahead adders. Carries ripple between the 4-bit adders.

   (c) A full carry-lookahead adder.

   What is the delay, in units of gate delays, for each of the three adders? Include figures showing the delay models you are using for the one-bit full adder, the four-bit carry-lookahead adder, and the carry-lookahead unit.

   How would the delays for your three adders generalize to an n-bit adder?

4. (10 pts.) The radix four digit set is, of course, $\{0, 1, 2, 3\}$. The *maximally* redundant signed digit radix four digit set is $\{\overline{3}, \overline{2}, \ldots, 3\}$. Show that it is possible to design an adder for this digit set, such that a carry propagates at most one digit position, by designing the addition table for the sum of two maximally redundant signed digit radix four digits. Hint: This is *far* easier than the radix two case.