Xilinx Tools Lab
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Mar. 7, 2008

1 Administrivia

Announcements

Assignment

Read 5.1–2.

From Last Time

Dataflow, hierarchical, behavioral VHDL design styles.

Outline

1. Introduction.

2. Lab.

Coming Up

Introduction to sequential circuits. Latches.
2 Introduction

For EX0R3 circuit demonstrate:

1. Library tab and set-up.
2. Syntax checking.
4. Testbench waveform.
5. Behavioral simulation and zooming.

3 Lab

1. Implement and simulate EX0R3.

   The source and library VHDL are on the class Web site. There are syntax errors in
   the source VHDL which you’ll need to find and fix.

2. Implement:
   
   (a) A 4-1 mux.

   (b) A hierarchical four-bit adder, using the fa component (see class Web site).

   (c) An eight-input priority encoder. This circuit has eight one bit inputs, one three
   bit output (the encoded value of the prioritized input), and a one bit valid output.

   Hint: a judicious use of don’t cares will make this quite easy to implement. The
   brute force approach requires a function table with $2^8$ entries!