Xilinx Test Programs

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This document will describe how to:

1. Run the test programs.
2. Assign pin constraints for problem 6-35.
3. Assign pin constraints for the second part of problem 6-21

Note: All reset signals are active low. This is contrary to the textbook. Deal with it.

1 Running the Test Programs

1. Download the two test driver programs from the class Web site. They are named `comp2.exe` and `handshake.exe`. Source code is available for your inspection.
2. Configure the FPGA with a bitstream. Then, open a command line window. Usually, you do this by selecting MSDOS prompt from the Programs menu. In the X Lab, from the Start menu open the Run box, type `command`, and press Enter.
3. Using `cd` in the command line window, navigate to the folder containing the executable test program. Type its name and press Enter. It will begin to run.

2 Pin Constraints for Problem 6-35

The optional active low reset signal is used for initialization.

Signal	Location
`clk_ext`	P50
`reset`	P48
`X`	P42
`Y`	P47
`Z`	P40

3 Pin Constraints for 2nd Part of Problem 6-21

Signal	Location
`clk_ext`	P50
`reset`	P48
`R`	P42
`A`	P47
`E`	P40