CPU16 Datapath and Control

Tom Kelliher, CS 240

May 3, 2006

1 Administrivia

Announcements

Assignment

From Last Time

CPU16 architecture.

Outline

1. CPU16 datapath.
2. CPU16 control.

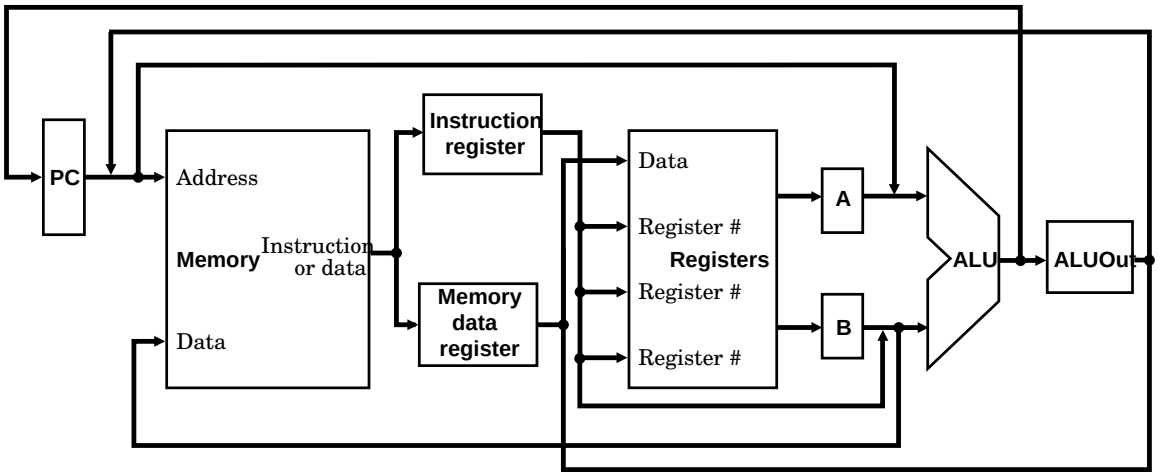
Coming Up

CPU16 implementation.

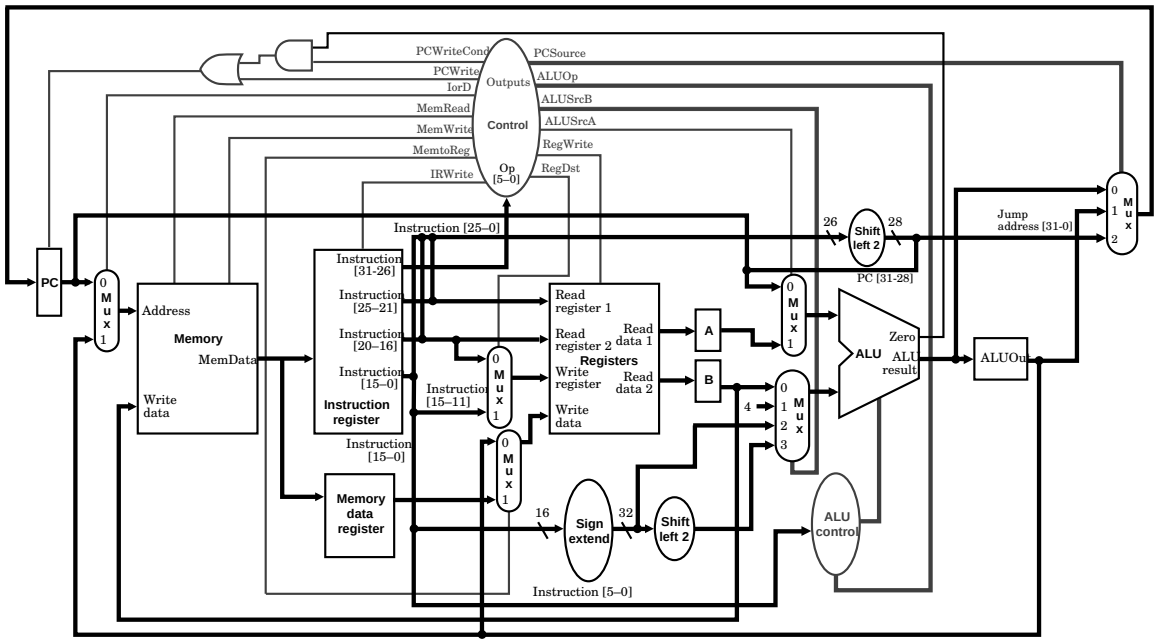
2 CPU16 Datapath

(To be modified according to our architecture.)

High-level block diagram:



3 The Complete Datapath



Control signals:

1. RegDst, RegWrite.
2. ALUSrcA: Choose between PC and Rs.
3. MemRead, MemWrite, MemtoReg.
4. IorD: Choose between PC and ALUOut for memory address.
5. PCWrite: Load a new value into PC.
6. PcWriteCond: Load a new value into PC if zero is active.
7. ALUOp.
8. ALUSrcB: Choose between Rt/Rd, 4, sign-extended immediate, sign-extended shifted immediate.
9. PCSource: Choose between PC + 4, ALUOut (branch target address), jump address

4 CPU16 Control

4.1 The Instruction Cycle

1. Steps: Fetch, decode, execution/completion.
2. Instructions: R-format, memory reference, conditional branch, jump.

4.1.1 Fetch

Common to all instructions.

1. Load IR.
2. Increment PC.

4.1.2 Decode

Common to all instructions.

1. Load A (rs field) and B (rt field) from register file.
2. Load ALUOut with branch target.

These are "optimistic" optimizations which *do no harm*, even if they are not needed/do not make sense for the current instruction.

4.1.3 Execution, Memory Address Computation, Branch Completion

Instruction classes go their own way.

1. R-format:
   (a) Perform ALU operation, loading ALUOut.
2. Memory reference:
   (a) Use ALU to compute sum of base & offset, loading ALUOut.
3. Conditional branch:
   (a) If `zero` load PC with computed branch target in ALUOut.

   This instruction has completed.
4. Jump:
   (a) Load PC with jump address.

   This instruction has completed.

4.1.4 R-Format Completion, Memory Access

Just two instruction classes remaining.

1. R-format:

   (a) Load register file (rd field) from ALUOut.

   This instruction has completed.

2. Memory reference:

   (a) sw: Memory location specified by address in ALUout written with value stored in B.

   This instruction has completed.

   (b) lw: MDR loaded from memory location specified by address in ALUOut.

4.1.5 LW completion

1. Load register file (rt field) from MDR.

4.2 Designing the Control Unit

Design the state machine necessary for controlling the datapath.