

Flip-Flops

Tom Kelliher, CS 220

Mar. 29, 2006

1 Administrivia

Announcements

Assignment

Read 6-4.

From Last Time

Sequential circuits and latches.

Outline

1. The problem with latches, again. Review of clocked SR latch.
2. Analysis of master-slave JK flip-flop.
3. Analysis of edge-triggered D flip-flop.
4. Characteristic tables.

Coming Up

Sequential circuit analysis.

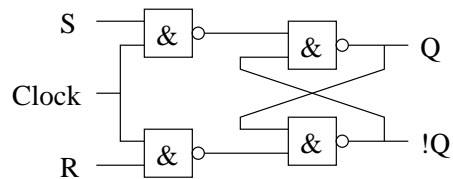
2 Problems with Latches

1. Level sensitivity, transparency.

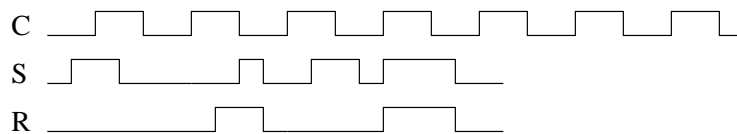
Must use two-phase, etc. clocking.

2. Solution: Flip-Flops, which remove transparency and permit use of a single clock signal

Clocked SR latch:



Analyze Q, !Q with these input waveforms. Assume Q low initially.

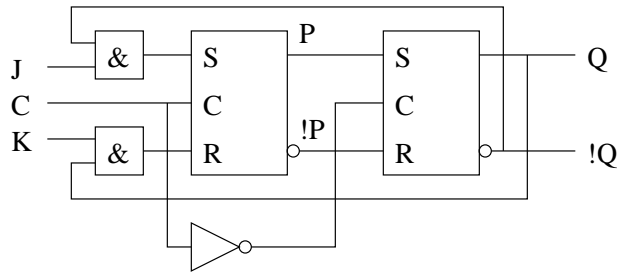


3 JK Flip-Flop

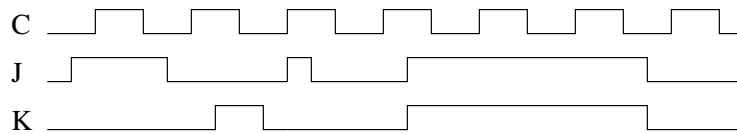
Master-Slave device: ensures no transparency. While master (leading latch) is transparent, slave is latched and vice-versa.

When J and K are both high, toggles in a controlled manner.

Diagram:



Analyze P, !P, Q, and !Q with these input waveforms. Assume Q low initially.

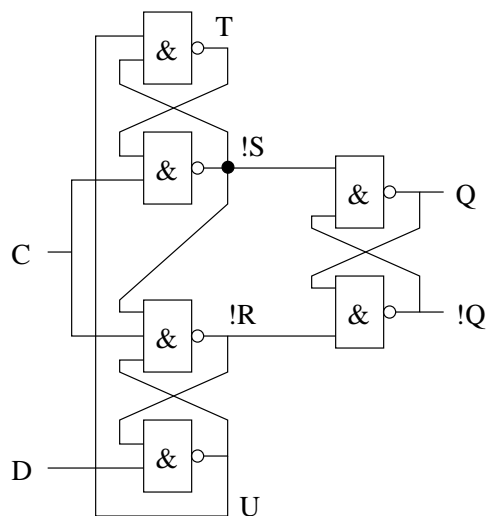


Changes state on edge, but not *edge*-triggered: one's catching.

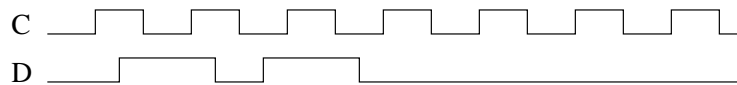
4 D Flip-Flop

Edge-triggered: samples input *only* during a clock transition.

Rising edge triggered D flip-flop. Figure 6-13 uses eight NAND gates and three inverters (verify for yourself). A slight improvement:



Analyze Q, !Q, !R, !S, T, and U with these input waveforms. Assume Q low initially.



Any one's catching?

5 Characteristic Tables

Compact way of representing flip-flop behavior.

1. JK flip-flop:

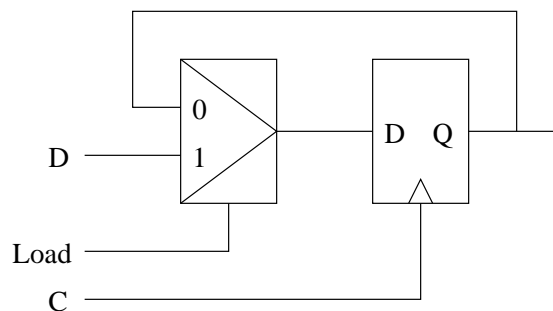
J	K	$Q(t+1)$	Operation
0	0	$Q(t)$	No change
0	1	0	Reset
1	0	1	Set
1	1	$\overline{Q(t)}$	Complement

Clock edge is implied in the transition from t to $t + 1$.

2. D flip-flop:

D	$Q(t+1)$	Operation
0	0	Reset
1	1	Set

Always loads. To control loading, use this circuit:



Gating the clock signal leads to problems.