Homework IV

Tom Kelliher, CS 240

50 points, due April. 3

1. 4-17. No credit will be given if you use any logic other than that mentioned in the problem.
2. 4-36. Turn in your simulation waveform and a justification of your testing procedure. You will be graded primarily on the test set you have chosen.
3. 4-45. Turn in your a listing of your VHDL code, your simulation waveform, and a justification of your testing procedure. You will be graded on the correctness of your VHDL as well as on the test set you have chosen.
4. 5-12. Hint: Design a modular one bit comparator. The idea is similar to that used to build an n-bit adder from n one-bit full adders.
5. Design three 64-bit adders:

   (a) A ripple carry adder using 64 one-bit full adders.

   (b) A partial carry-lookahead adder, using 16 4-bit carry-lookahead adders. Carries ripple between the 4-bit adders.

   (c) A full carry-lookahead adder.

   What is the delay, in units of gate delays, for each of the three adders? Be sure to clearly indicate the delay model you are using for a one-bit full adder, the four-bit carry-lookahead adder, and the carry-lookahead unit.

   How would the delays for your three adders generalize to an n-bit adder?
6. The radix four digit set is, of course, $\{0, 1, 2, 3\}$. The *maximally* redundant signed digit radix four digit set is $\{\overline{3}, \overline{2}, \ldots, 3\}$. Show that it is possible to design an adder for this digit set, such that a carry propagates at most one digit position, by designing the addition table for the sum of two maximally redundant signed digit radix four digits. Hint: This is *far* easier than the radix two case.