Combinational Logic; Hierarchical Design and Analysis

Tom Kelliher, CS 240

Feb. 17, 2006

1 Administrivia

Announcements

Assignment due now.

Assignment

Read 3.4.

From Last Time

IC technology.

Outline

1. Combinational logic.
2. Hierarchical design
3. Design analysis.

Coming Up

Design example.

2 Combinational Logic

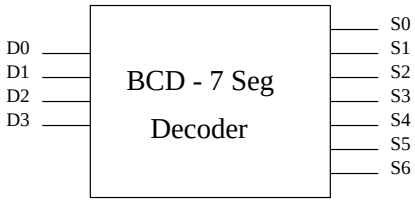
1. Definition: Logic circuits in which the output(s) depend solely upon current inputs.

2. No feedback or memory.

3. Sequential circuits: outputs depend upon current inputs *and* previous inputs.

   Memory or registers.

4. Example — BCD to 7-segment decoder:



3 Hierarchical Design

1. Intel's Pentium IV contains 42,000,000 transistors.

2. Design and conquer:

   CPU ⇒ Integer Unit ⇒ Adder ⇒ binary full adder ⇒ NAND gates

3. Reuse:

   Once logic is collected into a block, it can be instantiated several times in several places.

   Adders are used at several points within a CPU: integer ALU, program counter incrementer, multiplier, etc.

   Full binary adders are connected to form adders.

4. Scaling:

   Consider the two-dimensional tiling of memory cells.

These techniques reduce the number of transistors which must be laid out "by hand."

Design styles:

1. Top-Down design: divide and conquer.

2. Bottom-Up design: promotes reuse.

The savvy designer often uses both techniques within a single project.

Design tools:

1. CAD tools: programs to assist with schematic capture, HDL entry, synthesis, simulation. Running on "first silicon."

   The "old" days: drafting tables, taping out a circuit, and lots of prototyping.

2. HDLs and synthesis

   (a) Why VHDL is my favorite acronym.

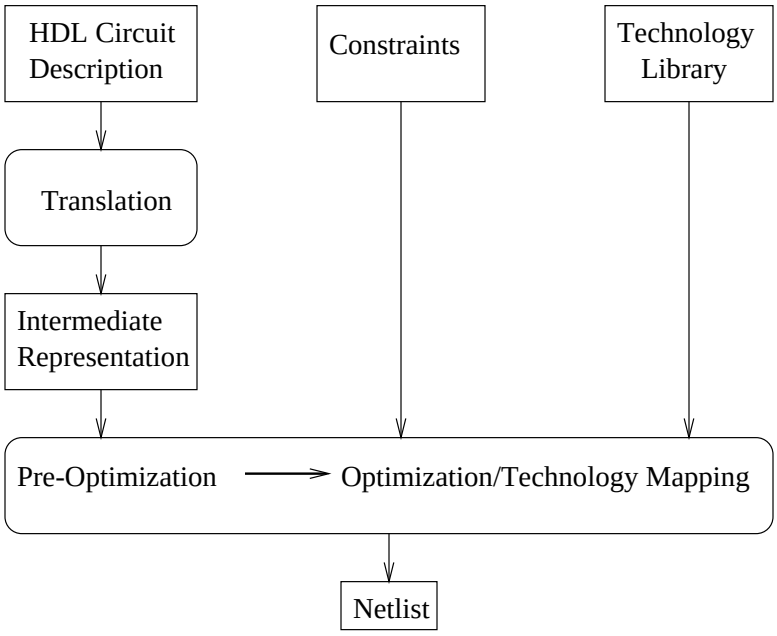
   (b) What is VHDL? 4-1 mux example:

```
library ieee;
use ieee.std_logic_1164.all;

entity mux4_1 is
   port (a0: in bit;
         a1: in bit;
         d0: in bit;
         d1: in bit;
         d2: in bit;
         d3: in bit;
         z: out bit);
end mux4_1;
```

```
architecture behavioral of mux4_1 is
signal address: bit_vector(1 downto 0);
begin
   address <= a1 & a0;
   with address select
      z <= d0 when "00",
           d1 when "01",
           d2 when "10",
           d3 when "11";
end behavioral;
```

(c) Synthesis process:



4 Design Analysis

Combinational circuit analysis — "reverse engineering." Skip.

Logic Simulation:

1. Vital today: First silicon must run.

   Can't re-wire a die.

Entire computers have been simulated to the point of booting the OS.

2. Simulator used to verify circuit behavior and timing.

   Results are only as good as the tests run.

   Large circuits cannot be simulated completely. Just ask Intel (`fdiv`).

3. Netlist used to describe circuit. Text file.

4. Schematic: graphical representation of circuit. Tool to convert to netlist form.

5. User produces "test vectors," which are the inputs to the simulator.

   Good test vectors are the key to meaningful results.