NAND, Two-Level Implementations, Parity

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Feb. 10, 2006

1 Administrivia

Announcements

Collect homework assignments.

Assignment

Read 2.8.

New homework assignment.

From Last Time

Simplifying K-maps.

Outline

1. NAND gates.
2. Two-level physical realizations.
3. Parity generation and checking.

4. BCD to 7-segment decoder example.

Coming Up

Circuit technologies.

2 NAND Gates

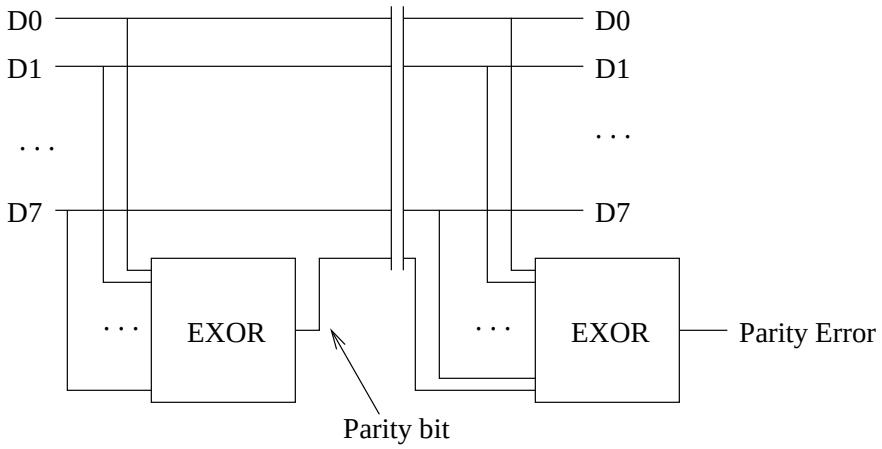
1. Not AND. Symbol. Truth table.
2. At the physical level, this is what we work with.
3. Completeness: Given a two-input NAND show how to implement inverter, AND, OR.
4. NOR completely analogous.

3 Physical Realizations

Given that we only have NAND gates, implement: $ABC + DEF + GHI$. (Draw using AND and OR, derive NAND implementation, and draw.)

4 Parity Generation and Checking

1. EXOR symbol, truth table.
2. EXOR = odd function. (NEXOR = even)
3. A "big" EXOR can be recursively constructed from "small" EXORs.
4. Parity generate and check circuit for ASCII data:



Show a few examples.

5 Example: BCD to 7-Segment Decoder

Simplify and implement S_4.