Multiplier Functional Unit

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1 Administrivia

Announcements

Assignment

From Last Time

Counters.

Outline

1. Brief description of surrounding system.

2. Multiplier datapath.

3. Adding control to the datapath.

Coming Up

VHDL for multiplier.


2 Surrounding System

1. In CS 220, we studied a single-cycle implementation. Here, we need a multi-cycle implementation, to handle the multiplier and memory access.

2. Assume multiplier and multiplicand are provided during the same clock cycle. The result is stored in two registers: High and the named destination register.

   Assembly example:

   \[
   \text{mul } \text{s2}, \text{s1}, \text{s0}
   \text{mvh } \text{s3}
   \]

3. We need a “start” signal and a “done” signal.

3 Multiplier Datapath

The standard optimized shift and add multiplier. What’s its running time?

How/why does this work?

Will this work for negative values?
4 Adding Control

Assume a 16-bit adder. Let’s get started.