# Controlling the Flow-Through Processor

Tom Kelliher, CS 220

## 1 Administrivia

### Today's Objectives

1. Understand control of the flow-through processor.

### Next Up

Read 7.3

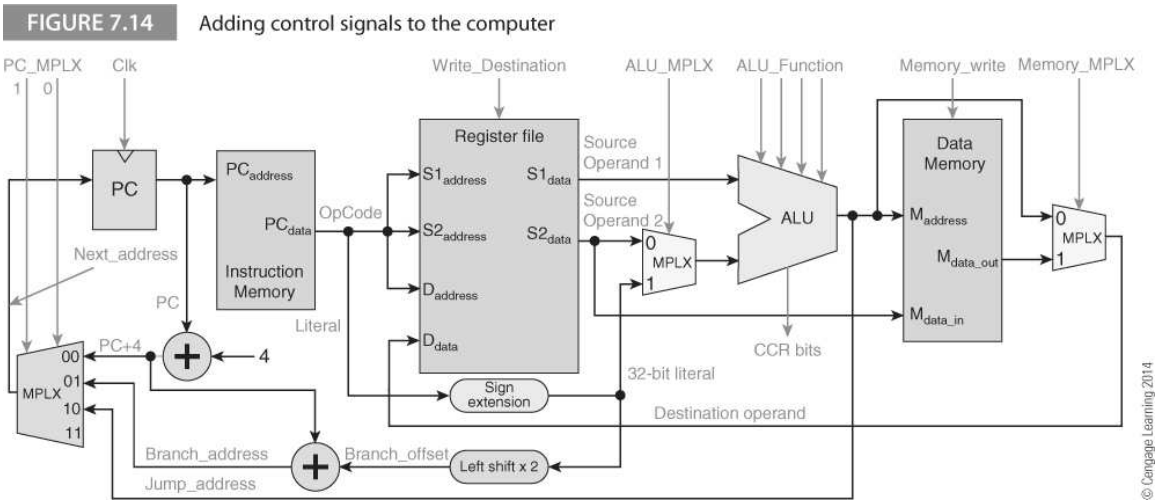
1. Calculate the speed-up advantage of pipelining.
2. Discuss implementation issues involved with pipelining.
3. Understand pipeline hazards

# 2 Warm-Up

1. Decode the following ARM instruction and indicate the data path control signal values for executing it.

   `0X12933001`

   Use the ARM Instruction Set Data Sheet on the class home page.



2. As you'll see in the problem set, such control signal values have to be generated for each instruction execute. The circuit that generates these control signals takes opcodes as inputs, and produces the control signal values as ouptputs. Which of the following types of circuits could be used to generate produce these signals?

   (a) Decoders

   (b) A memory

   (c) A large combinational logic circuit

   (d) (a) and (b)

   (e) (b) and (c)

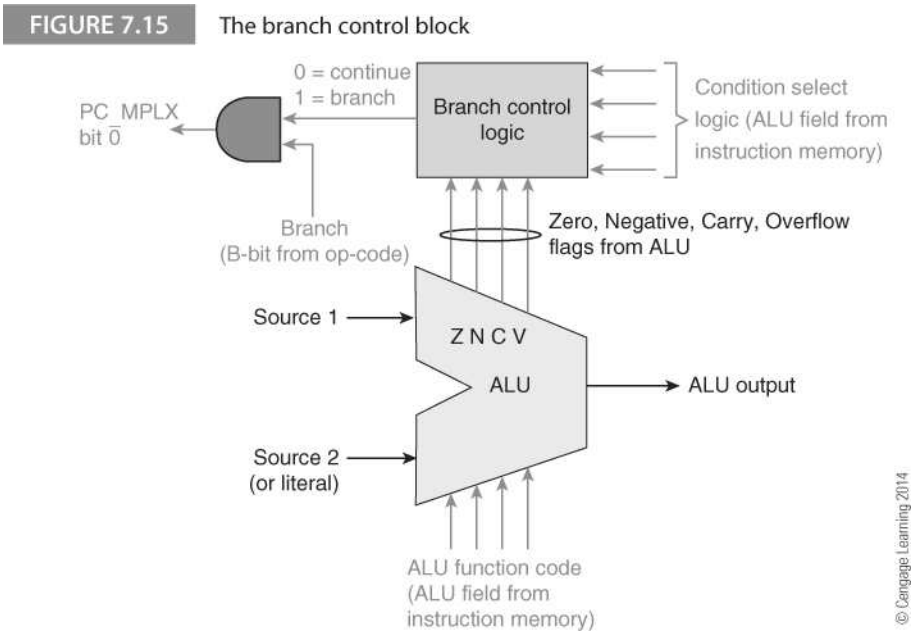
# 3 Problem Set 13.0

1. Decode the following ARM instructions and indicate the data path control signal values for executing them.

   ```
   0XE7940005
   0XE5880014
   0X0AFFFFFB
   ```

2. Looking at the ARM instruction set formats on pg. 4-2 of the ARM Instruction Set Data Sheet, and thinking about how you decoded the instructions in the previous problem, which bits of an instruction are the opcode bits? Explain.

3. Consider the following figure from the textbook:




   The note underneath the Branch input to the AND gate states that there is a B-bit in the opcode. There doesn't appear to be such a bit. Write the Boolean equation that would indicate that a branch instruction is being executed.