The Stored Program Machine: A Closer Look

Tom Kelliher, CS 220

1 Administrivia

Today's Objectives

1. Demonstrate an understanding of the structure and components of the hypothetical stored program machine by explaining the purpose of each component and tracing the fetch and execution stages of simple instructions through the machine.

2. Determine the effect of these ISA features on instruction size: registers, addressing modes, and instruction format.

Next Up

Read 3.3–3.5, pp. 1–5 of the *Graded ARM Assembly Language Examples* document on the course web site, and view the *Keil uVision4 How-to* video linked-to from the course web site. You will be modifying, assembling, and running ARM programs during class; pay close attention while watching the video, re-watching it and taking notes as necessary.

1. Begin to familiarize yourself with the ARM ISA.

2. Learn the structure of an ARM program and use Keil uVision4 to assemble and run simple ARM programs.

3. Understand and use ARM data-processing instructions.

2 Warm-Up

1. The hypothetical stored program machine component that points to the current instruction is the

   (a) Memory address register

   (b) Memory buffer register

   (c) Program counter

   (d) Instruction register

   (e) None of the above.

2. Register file registers hold

   (a) Data

   (b) Data and addresses

   (c) Addresses

   (d) Instructions

   (e) Data, addresses, and instructions

3. In the following sequence of RTL statements, which statement reads an instruction from memory?

```
(a) [MAR] <- [PC]
(b) [PC] <- [PC] + 4
(c) [MBR] <- [[MAR]]
(d) [IR] <- [MBR]
```

4. The CCR should be updated

   (a) never

   (b) always

   (c) prior to executing a conditional branch

   (d) whenever the assembler tells us

5. Which of the following is not an addressing mode?

   (a) Literal

   (b) Register

   (c) Direct

   (d) Indirect

   (e) None of the above.

3 Problems

1. Write RTL to implement

   ```
   STR r1, 1234
   ```

2. Write RTL to implement

   ```
   ADD r0, r1 #1234
   ```

3. For each of the following six-bit operations, calculate the values of the C, Z, V, and N flags.

   (a) $001011 + 001101$

   (b) $111111 + 000001$

   (c) $000000 - 111111$

4. Describe the effect of making the following ISA modifications on instruction size and program size. Consider each modification individually.

   (a) Adding additional general purpose registers.

   (b) Adding more instructions.

   (c) Enlarging the address space.

   (d) Adding direct addressing.

   (e) Changing from a three-address machine to a one-address machine.