

Xilinx Test Programs

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This document will describe how to:

1. Run the test programs.
2. Assign pin constraints for problem 4-42.
3. Assign pin constraints for problem 4-43.

Note: All reset signals are active low.

1 Running the Test Programs

1. Download the two test driver programs from the class Web site. They are named `comp2.exe` and `handshake.exe`. Source code is available for you to look at.
2. Configure the FPGA with a bitstream. Then, open a command line window. Usually, you do this by selecting MSDOS prompt from the Programs menu. In the X Lab, from the Start menu open the Run box, type `command`, and press Enter.
3. Using `cd` in the command line window, navigate to the folder containing the executable test program. Type its name and press Enter. It will begin to run.

2 Pin Constraints for Problem 4-42

Signal	Location
<code>clk_ext</code>	P50
<code>reset</code>	P48
<code>X</code>	P42
<code>Y</code>	P47
<code>Z</code>	P40

3 Pin Constraints for Problem 4-43

Signal	Location
<code>clk_ext</code>	P50
<code>reset</code>	P48
<code>R</code>	P42
<code>A</code>	P47
<code>E</code>	P40