

# Inside RAM

Tom Kelliher, CS 220

Nov. 25, 2003

## 1 Administrivia

**Announcements**

**Assignment**

**From Last Time**

Review of exam and discussion of counter project.

**Outline**

1. Introduction.
2. Static RAM.
3. Dynamic RAM.

**Coming Up**

Review for final.

## 2 Introduction

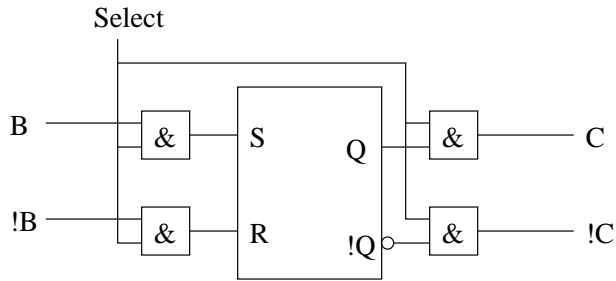
1. Organizations of RAMs: number of words, bits/word.
2. Operation:
  - (a) Not enabled: low power mode, output in high-impedance state (disconnected)
  - (b) Read: A single word should be read. Address may change.
  - (c) Write: A single word should be written. Address must be stable.
  - (d) Refresh. Hidden or not hidden?
3. RAM will have a 2-D structure: row/word, column/bit.

The number of columns may not have anything to do with bits/word — many RAMs have 1 bit/word but are 2-D internally.

4. RAMS consist of:
  - (a) Storage cells.
  - (b) Word and bit decoders.
  - (c) Write logic.
  - (d) Read logic (sense amp).
  - (e) Refresh logic for DRAMs.

## 3 Static RAM

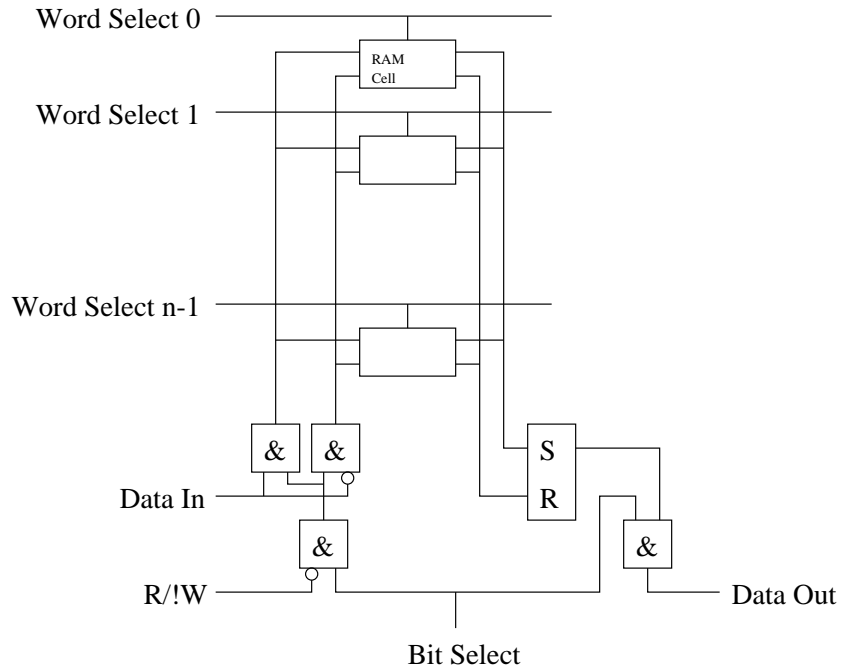
1. Memory cell model:



Goal: cell should be as small as possible, to increase storage density.

Think about the AND gates on the output side as tri-state buffers — transmission gates.

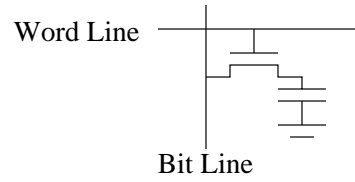
2. Bit slice of a RAM array:



3. Assume you have  $4 \times 1$  bit-slice RAM cells. Adding 2-to-4 decoders, how would a  $4 \times 4$  RAM look? A  $16 \times 1$  RAM?

## 4 Dynamic RAM

1. DRAM cell:



2. SRAM cell: five or six transistors. DRAM cell: one transistor and one capacitor.
3. Bit-Slice: support structure similar.
4. Bit line has higher capacitance than storage capacitor — sense amps.
5. *Destructive* read. Use of sense amps to restore data.
6. Refresh due to leakage. Refresh logic.