Homework IV

Tom Kelliher, CS 220

50 points, due Nov. 3

On pp. 173–179:

1. 3-23. Other than the three 4-1 muxes, no additional logic is needed.

2. 3-37.

3. 3-42. Show all work, including your verification.

4. 3-47. Design a one bit comparator. Then, use a modular approach, similar to that taken when building an n-bit adder from n one bit full adders.

5. 3-55. Turn in your simulation waveform and a justification of your testing procedure. You will be graded primarily on the test set you have chosen.

6. 3-64. Turn in your a listing of your VHDL code, your simulation waveform, and a justification of your testing procedure. You will be graded on the correctness of your VHDL as well as on the test set you have chosen.