Implementing a Xilinx Project

Tom Kelliher, CS 220

Fall, 2001

So, you've synthesized your VHDL design and now it's time to "burn" it into the hardware. This document will take you through that process using the Xilinx and Xstools software:

- Required VHDL code for clock signals. **Do this before synthesizing.**

- Implementing your design.

- Timing simulation.

- Adding pin constraints to your design and creating a new version.

- Testing the FPGA board (Xstools).

- Downloading a bit stream into the FPGA board (Xstools).

I assume you have a synthesized design upon which you've performed functional simulation.

1 Required VHDL Code for Clock Signals

Due to their importance, clock signals require special handling. You will need to add the following to your VHDL code. I will assume that you named your external clock signal (the name given in the port list of the entity declaration) `clk_ext`. Otherwise, modify the following for your naming convention. Add the following to the declarations section of your architecture body:

```
component ibuf port (
  i : in  std_logic;
  o : out std_logic);
end component;

component bufg port (
  i : in  std_logic;
  o : out std_logic);
end component;

signal clk_pad, clk : std_logic;
```

Add this to the body of your architecture:

```
u1 : ibuf port map (
  i => clk_ext,
  o => clk_pad);
```

```
u2 : bufg port map (
  i => clk_pad,
  o => clk);
```

The clock signal that you will now use to control your flip-flops is `clk`.

2   Implementing a Design

1. In the flow window, click the Implementation button.

2. A Synthesis/Implementation settings dialog box will pop up. Verify the settings and click Run.

3. The Flow Engine will now run to create your bit file. You get to watch the various implementation stage programs run. If all goes well, all of them will complete successfully and you will have a bit stream file.

4. You will need to add pin constraints before downloading your design into the FPGA.

3   Timing Simulation

Once you've implemented a design, you can run a timing simulation. In the flow window, click on the left button within the Verification step. The timing simulation tool is quite similar to the functional simulation tool, which you've already used. The major differences are that the timing simulation tool will show you actual propagation delays between signals and flip-flop asynchronous resets will function correctly. (Reset does not work under functional simulation.)

One consequence of the propagation delays modeled by the timing simulator is that you must allow flip-flop D inputs to settle before clocking the flip-flops. In other words, change the flip-flop input values, do a simulation step, then bring the clock high.

4   Adding Pin Constraints and Creating a New Version

1. You must implement a design before adding constraints.

2. Open the Tools menu, choose Implementation, then choose Constraints Editor.

3. The Constraints Editor will open.

4. Choose the ports tab and enter location values for your I/O signals. (You will be told separately what these location values should be for the homework problems.) Press the Enter key after entering each location and verify that the new constraint is visible in the UCF Constraints window at the bottom of the editor.

   Be careful when filling in this information. Doing this incorrectly can result in damage to the FPGA board, the PC, or both. Not to mention what it will do to your wallet!

5. Save the constraints and exit the editor. You will receive a message reminding you to re-run the translate step. This is normal.

6. So that the constraints don't get deleted if your re-synthesize and re-implement, you need to create a new version of the design. Open the Project menu and choose Create Version. A Create Version dialog box will open. If not already filled-in, set the Version Name to ver2. Re-check your target device settings, and click Run.

7. Now, implement your design a second time. When the implementation completes, click the Reports tab and then double-click the Implementation Report Files folder. The Report Browser will open up. Open the Pad Report and verify that the pad constraints are correct. Do not proceed if they aren't correct. Do not pass Go and do not collect $200. Go back to the Constraints Editor and correct your mistakes.

Note: Any time you modify the constraints, you will have to create a new version of the design. Don't forget to increment the version number.

5 Testing the FPGA Board

You can do this to verify that the board is functioning correctly.

- From the Start menu, go to Programs, then Xstools, then choose gxstest.

- Set Board Type to XS40-010XL and Port to LPT1.

- Press the TEST button. The test will run. A successful completion is indicated by the number zero being displayed on the seven-segment display. Prior to that, the display will flicker. This is normal.

6 Downloading a Bit Stream

1. Open your design folder and locate your bit stream file. It will have a `.bit` extension.

2. From the Start menu, go to Programs, then Xstools, then choose gxsload.

3. Make sure that Port is set to LPT1.

4. Drag your bit stream file into the Recent Files area of the gxsload application. Gxsload will download the bit stream into the FPGA.

5. You're now ready to use the FPGA.