

Introduction to Sequential Logic; Latches

Tom Kelliher, CS 220

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1 Administrivia

Announcements

Assignment

Read 4-3.

Homework due in one week: lab tutorials; complete VHDL problems during the week. For VHDL problems: hand-in VHDL print-out and simulation results from Xilinx tools. Sign-up sheets for workstation time?

From Last Time

Finished introduction to VHDL. See course web page for VHDL code.

Outline

1. Sequential logic.
2. SR latch.
3. D latch.

Coming Up

2 Sequential Logic

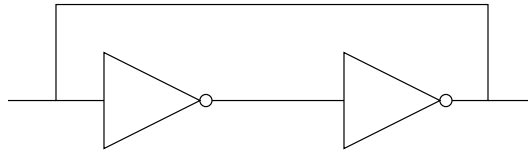
1. Combinational logic is nice but...
2. Sequential logic: introduces notion of memory.
3. Synchronous vs. asynchronous circuits.

There will all be some asynchronous elements in a circuit which interfaces to the real world environment.

4. Clock: frequency, period, edges, duty-cycle.

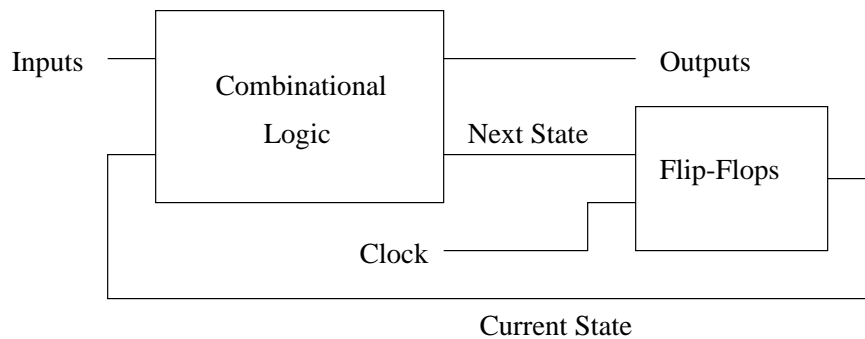
Non-overlapping clocks.

5. How can we achieve memory?



This is the basic idea, to be modified for actual use.

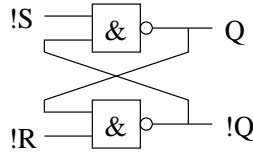
6. General model of a sequential circuit:



3 SR Latch

1. Active low inputs.

2. Schematic:

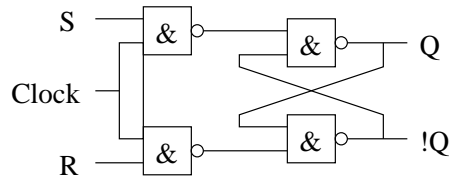


3. Operation: three valid, one invalid input.

4. Asynchronous.

3.1 Clocked SR Latch

1. Schematic:



Behavior.

2. Transparent when clock is high.

Latched when clock is low.

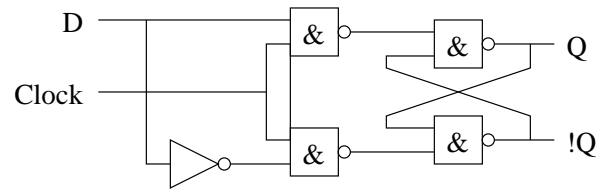
3. Problem with use in circuits: double clocking.

A solution: non-overlapping clocks. (Achieved with master-slave flip-flops.)

4 D Latch

1. SR latches inconvenient when storing data from, say, an ALU.

2. D latch stores data directly:



(Think of this as a logic primitive.)