Sequential Circuit Design

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1 Administrivia

Announcements

Shall we push-off the exam until we've finished Chapter 4?

Assignment

Read 4-8.

Homework due 11/12: 4-20, 4-21, 4-42, 4-43. For the last two, you will download your designs to an FPGA board and run a program I will provide to test your circuits.

From Last Time

Sequential circuit analysis.

Outline

1. Sequential circuit design process.
2. Unused states.
3. Examples.

Coming Up

VHDL for sequential circuits.

2 Sequential Circuit Design Process

1. Obtain a state diagram. Assign binary numbers to the states (a non-trivial problem, actually).

2. Obtain a state table.

3. Derive flip-flop input equations from the next state entries and output equations. Simplify.

4. Draw your schematic.

3 Unused States

Suppose your design has 6 states:

1. Two unused states.

2. What happens if the circuit enters one of these states?

4 Examples

1. Sequence recognizer for 010.

2. Serial comparator. Inputs: A, B, msb. A and B are received least significant bit first. Receipt of msb is co-incident with msb's of A and B and resets circuit to begin next comparison. Output 0 if A $\geq$ B, otherwise 1.

3. Serial comparator. Inputs: A, B, lsb. A and B are received most significant bit first. Receipt of lsb is co-incident with lsb's of A and B and resets circuit to begin next comparison. Output 0 if A $\geq$ B, otherwise 1.